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Third Semester B.E. Degree Examination, June/July 2019 Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain with help of a circuit diagram and characteristic curves working of N-channel Enhancement – MOSFET (E-MOSFET) (10 Marks)
- b. Explain any two applications of field Effect Transistor (FET) along with the circuit diagram. (06 Marks)

OR

- 2 a. Explain the operation of Astable multi-vibrator with a neat diagram. (08 Marks)
- b. Explain performance parameters of operational amplifiers. (08 Marks)

Module-2

- 3 a. Describe positive and negative logic. list the equivalences between them. (04 Marks)
- b. Simplify the following boolean function using k-map method.
 $F(A, B, C, D) = \pi M(0, 1, 2, 4, 5, 10) + d(8, 9, 11, 12, 13, 15)$
 Get the simplified POS form of k-map. (04 Marks)
- c. What is a Hazard? Explain Static – 0 hazard and its Hazard cover. (08 Marks)

OR

- 4 a. Give simplified logic equation using Quine-McClusky method for the following Boolean function $F(A, B, C, D) = \sum m(0, 3, 5, 6, 7, 11, 14)$. (12 Marks)
- b. Mention the different verilog HDL model and write the verilog HDL code using structural model for the circuit given in Fig Q4(b)

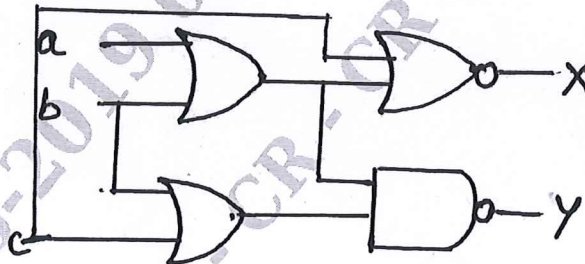


Fig Q4(b)

(04 Marks)

Module-3

- 5 a. Implement the following function using 8:1 multiplexer
 $F(A, B, C, D) = \sum m(0, 1, 5, 6, 8, 10, 12, 15)$ (06 Marks)
- b. Show that using a 3:8 decoder and multi-input OR gate, the following boolean expression can be realized $F_1(A, B, C) = \sum m(0, 4, 6)$
 $F_2(A, B, C) = \sum m(1, 2, 3, 7)$ (04 Marks)
- c. Design even parity generator. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and/or equations written eg. 42+8 = 50, will be treated as malpractice.

OR

- 6 a. Design seven segment decoder using Programmable Logic Array (PLA) (08 Marks)
b. What is Magnitude comparator? Design one bit comparator using basic gates? (08 Marks)

Module-4

- 7 a. Explain the working of a JK master – slave Flip – Flop along with its implementation using NAND gates. (08 Marks)
b. Draw the state transition tables of JK, T, D and SR Flip – Flops. (08 Marks)

OR

- 8 a. Explain a 4-bit serial – In – Serial – out (SISO) registers using negative edge triggered D-Flip-Flops. Draw the waveform to shift binary number 1111 into this register. (08 Marks)
b. Write the comparison between synchronous and asynchronous counter. (04 Marks)
c. Explain Ring counter with a neat diagram. (04 Marks)

Module-5

- 9 a. Define counter. Design and Implement a MOD – 5 synchronous counter using JK Flip-Flop. (10 Marks)
b. With a neat diagram explain Digital clock. (06 Marks)

OR

- 10 a. Explain 2 bit simultaneous A/D converter. (10 Marks)
b. Explain the Binary ladder with digital input of 0100. (06 Marks)
