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10ES33

Third Semester B.E. Degree Examination, Dec.2017/Jan.2018
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Represent the canonical minterm forms in decimal notation :

i) $f_1 = x\bar{y} + yz$

ii) $f_2 = \bar{a}c + bc\bar{d} + ad$. **(05 Marks)**

b. Show that f(a, b, c, d) = ∑m(0, 1, 2, 5, 6, 8, 9, 10, 13, 14) = πM (3, 4, 7, 11, 12, 15). **(08 Marks)**

c. Simplify the following Boolean function and realize the simplified expression using basic gates.
f(a, b, c, d, e) = ∑m(0, 1, 4, 8, 9, 11, 15, 16, 24, 26) + dm(10, 20, 22, 23, 25, 27, 31). **(07 Marks)**

2 a. Simplify the Boolean function f(a, b, c, d) = ∑m(0, 1, 2, 7, 8, 9, 10, 13, 15) using Quine – Mc Cluskey tabulation method and verify the answer using k-map. **(10 Marks)**

b. Simplify the Boolean function f(a, b, c, d) = ∑m(0, 2, 3, 4, 5, 8, 10, 11) + dm(7, 13, 14) using Map entered variable k-map. With "d" as map entered variable, verify the answer using k-map,. **(10 Marks)**

3 a. Design a combinational circuit using basic gates to convert excess 3 binary code to BCD code. **(10 Marks)**

b. Implement full adder using decoder. **(05 Marks)**

c. Design a 4 to 16 decoder using 3 to 8 decoders. **(05 Marks)**

4 a. Design a 4 bit BCD adder circuit using 7483IC with self correcting circuit. That is a provision to be made in the circuit, in case the sum of BCD exceeds 9. **(10 Marks)**

b. Realize the Boolean function f(a, b, c) = ∑m(0, 1, 4, 5, 6) using 4 : 1 mux. **(05 Marks)**

c. Explain look – ahead carry adder and give its advantages and disadvantages. **(05 Marks)**

PART – B

5 a. Obtain characteristic equation of a S-R flip-flop. **(05 Marks)**

b. Explain the working of an universal shift register. **(05 Marks)**

c. Explain the working of a master –slave JK flip-flop with timing diagram for master and slave. Show how race around condition is eliminated. **(10 Marks)**

6 a. Design an asynchronous mod-8 counter using JK flip-flop and draw its timing diagram. **(10 Marks)**

b. Explain why asynchronous counter is called ripple counter. **(05 Marks)**

c. Explain mealy and Moore sequential circuit models. **(05 Marks)**

7 a. Draw and explain Moore JK flip-flop state diagram. **(05 Marks)**

b. For the state machine shown Fig.Q7(b) obtain : i) state table ii) Transition table iii) excitation table for JK flip–flop iv) logic diagram. **(15 Marks)**

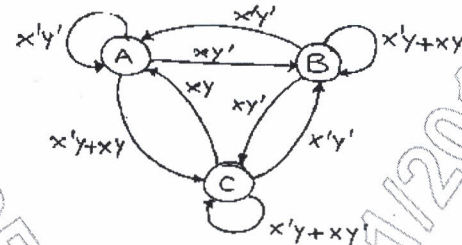

Fig.Q7(b)

8 a. Design a cyclic BCD up synchronous counter using T flip-flops. **(10 Marks)**

b. Design a cyclic synchronous counter using D flip-flops to generate a sequence of 5421 code. (Hint : 0, 1, 2, 3, 4, 8, 9, 10, 11, 12 0, 1 - - - -) sequence. **(10 Marks)**

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