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10EE764

Seventh Semester B.E. Degree Examination, Dec.2017/Jan.2018
VLSI Circuits and Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With neat diagrams explain the operation of enhancement mode nMOS transistor with different V_{ds} voltages. **(06 Marks)**

b. Explain CMOS p-well fabrication process with neat diagrams. **(09 Marks)**

c. Compare CMOS and biopolar technologies. **(05 Marks)**

2 a. Show that pull-up to pull-down ratio for nMOS inverter driven thro' one or more pass transistor is 8:1. **(08 Marks)**

b. Explain Latch-up in CMOS circuits with relevant diagrams and waveforms. **(06 Marks)**

c. Define MOS transistor trans-conductance and output conductance and derive expression for g_m and g_{ds}. **(06 Marks)**

3 a. With relevant diagrams explain Lambda (λ) based design rules as applicable to wires and transistors. **(08 Marks)**

b. Draw the circuit symbol and stick diagrams for CMOS inverter. **(05 Marks)**

c. Draw the stick diagram and layout for nMOS shift register cell. **(07 Marks)**

4 a. What is sheet resistance? Calculate sheet resistance for transistor channel if L = 8λ, w = 2λ and n-channel $R_s = 10^4$ Ω/square. **(04 Marks)**

b. With schematic diagrams explain inverting and non inverting super buffers. **(08 Marks)**

c. Explain three different kinds of wiring capacitances. **(08 Marks)**

PART – B

5 a. Derive scaling factor for any ten device parameters. **(10 Marks)**

b. Discuss the limitation of scaling on interconnect and contact resistance. **(10 Marks)**

6 a. Draw the stick diagram for 2-input CMOS NAND gate. **(05 Marks)**

b. Explain in detail Pseudo- nMOS logic taking inverter as an example. **(07 Marks)**

c. With block diagram and stick diagram explain the design approach of a parity generator. Using nMOS logic. **(08 Marks)**

7 a. Draw and explain combinational circuit to generate two phase clocking. **(06 Marks)**

b. Explain percharge bus concept with relevant diagrams. **(06 Marks)**

c. Explain the operation of 4×4 cross bar switch with neat diagram. **(08 Marks)**

8 a. Explain implementation of ALU functions with an adder using appropriate figures and expressions. **(10 Marks)**

b. Draw the structure of multiplexer based adder logic with stored and buffered sum output and explain. **(10 Marks)**

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