CBCS SCHEME

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15EE35

Third Semester B.E. Degree Examination, June/July 2018
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Define combinational logic, canonical SOP and canonical POS, with examples. **(06 Marks)**

b. Place the following equations into proper canonical form:

i) $R = f(a,b,c) = (\bar{a}+b)(b+\bar{c})$ into minterm canonical form.

ii) $Z = f(a,b,c) = a + \overline{\bar{a}b}$ into maxterm canonical form. **(04 Marks)**

c. Solve the following Boolean equation using four variable Karnaugh map and implement the simplified equation using minimum number of logic gates.
$f(a, b, c, d) = \sum (0, 5, 7, 8, 10, 13) + d (2, 4, 14, 15)$. **(06 Marks)**

OR

2 a. Solve four variable expression using Quine McCluskey minimization technique.
$K = f(a,b,c,d) = \pi M(0,3,4,7,8,10,12,14) + d(2,6)$ **(08 Marks)**

b. Simplify the Boolean expression using a 3-variable VEM, with 'Z' as MEV
$f(w, x, y, z) = \sum m (3, 4, 5, 7, 8, 11, 12, 13, 15)$. **(08 Marks)**

Module-2

3 a. Implement 3-bit binary to gray code conversion circuit using IC 74139. Draw neat diagram, truth table with switching equations in SOP form. **(06 Marks)**

b. Implement the following multiple output functions for active low outputs using IC74138.
$F_1 = f(x,y,z) = \bar{x}y + xy\bar{z} + xz$, $F_2 = f(x,y,z) = \pi(0,1,4,5,7)$. **(04 Marks)**

c. What are multiplexers? Implement the function using 8:1 MUX,
$f(a, b, c, d) = \sum m(0, 1, 3, 4, 7, 10, 11, 14, 15)$. **(06 Marks)**

OR

4 a. Implement 4-bit parallel adder/subtractor using 4-full adder blocks. If $C_{in} = 0$ the circuit should act as adder and if $C_{in} = 1$ the circuit should act as substractor. Explain its operation by considering examples. **(06 Marks)**

b. What is the problem associated with the parallel adder? Explain the method of correcting it, with suitable circuit and equations. **(06 Marks)**

c. Design 1-bit comparator circuit, represent truth table, K-maps and logic diagram. **(04 Marks)**

Module-3

5 a. Explain the operation of Master-Slave JK flip-flop with logic diagram, truth table, symbol and timing diagram. **(08 Marks)**

b. Distinguish between sequential circuits and combinational circuits. **(04 Marks)**

c. Explain the operation of basic bistable element, using two-inverter configuration. **(04 Marks)**

OR

6 a. Derive characteristics equations for SR flip-flop and JK flip-flop, represent truth table and K-maps. **(04 Marks)**

b. Explain the operation of 4-bit ring counter and twisted ring counter. **(06 Marks)**

c. Design synchronous MOD6 counter using clocked 'D' flip flops for the sequence $0 \rightarrow 2 \rightarrow 3 \rightarrow 6 \rightarrow 5 \rightarrow 1$, again, 0.... represent application table, excitation table and logic diagram. **(06 Marks)**

Module-4

7 a. Define state variables and excitation variables and write a note on Moore and Mealy sequential models. **(08 Marks)**

b. For the logic diagram shown in Fig.Q.7(b), find excitation table, state table and state diagram. **(08 Marks)**

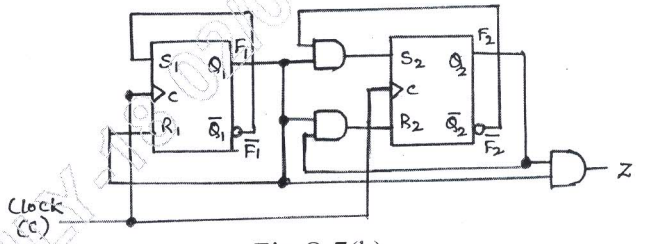

Fig.Q.7(b)

OR

8 a. Analyze the circuit shown in Fig.Q.8(a), obtain excitation table, state table and state diagram. **(10 Marks)**

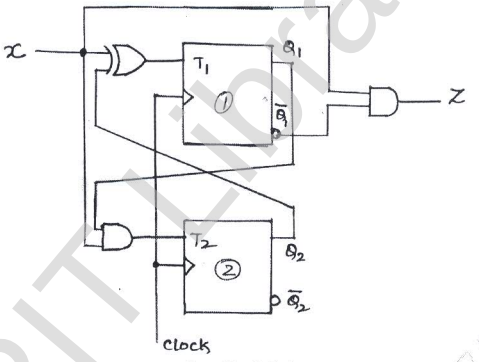

Fig.Q.8(a)

b. Design the sequential logic circuit for single input single output system shown in Fig.Q.8(b) state diagram using clocked 'D' flip-flop. **(06 Marks)**

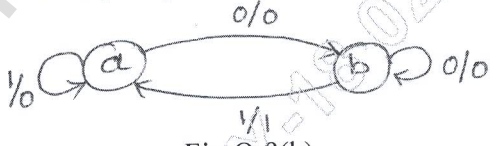

Fig.Q.8(b)

Module-5

9 a. Explain the structure of VHDL and verilog module with example code for each and compare them. **(08 Marks)**

b. List the various styles/types of descriptions in VHDL and verilog. Explain VHDL structural description with example code. **(08 Marks)**

OR

10 a. Explain the structure of data flow description in VHDL and verilog, using suitable example code. **(08 Marks)**

b. Write VHDL and verilog code for 2 × 2 magnitude comparator for all input combinations. **(08 Marks)**

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