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BANGALORE - 560 037

10EE764

**Seventh Semester B.E. Degree Examination, June/July 2018**  
**VLSI Circuits and Design**

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions, selecting  
at least TWO questions from each part.**

**PART – A**

- 1 a. Explain in detail, the process of n-MOS fabrication with the help of necessary fabrication structures. (10 Marks)
- b. Discuss Moore's law. Explain the working of enhancement mode of transistor with different values of  $V_{ds}$ . (10 Marks)
- 2 a. Derive an expression for  $I_{ds}$  for both saturated as well as non saturated region. (10 Marks)
- b. Define  $Z_{pu}/Z_{pd}$ . Show that pull up to pull down ratio for nMOS inverter driven through one or more pass transistor is 8 : 1. (10 Marks)
- 3 a. Draw the monochrome stick diagram of n-MOS shift register cell. (06 Marks)
- b. Define stick diagram. Explain the encoding used for simple n-MOS process. (06 Marks)
- c. What are the advantages of complementary transistor pull-up for an inverter? With relevant diagram, explain the CMOS inverter operation in different region. (08 Marks)
- 4 a. Define sheet resistance, square capacitance and delay unit, explain it same for different technologies. (06 Marks)
- b. Estimate CMOS inverter delay interms of rise time and fall time. (06 Marks)
- c. Calculate the total capacitance in picofarads between the substrate and structure as shown in Fig. Q4 (c) for  $\Lambda = 5 \mu\text{m}$ . Use standard values. (08 Marks)

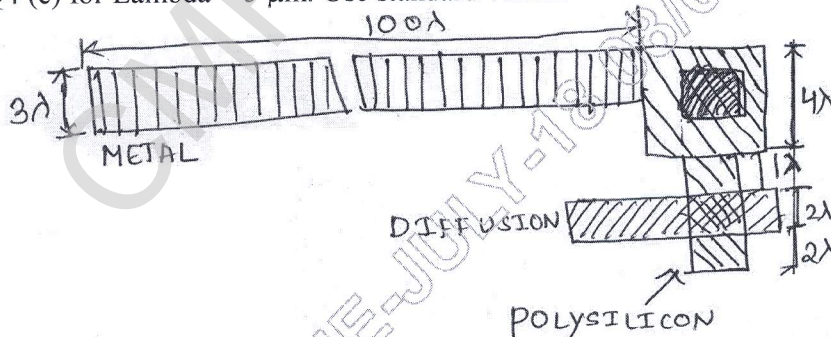


Fig. Q4 (c)

**PART – B**

- 5 a. Derive the scaling factors for the following device parameter by considering constant electric field scaling model:
  - (i) Gate capacitance
  - (ii) Maximum operating frequency
  - (iii) Current density.
  - (iv) Channel resistance.
  - (v) Power dissipation per gate  $P_g$ . (10 Marks)
- b. Discuss in detail the limitation of scaling and limits due to subthreshold currents. (10 Marks)

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- 6 a. Write the structure and stick diagram of nMOS, CMOS 2 I/P nand gates. (06 Marks)  
b. Prove that for pseudo nMOS logic  $Z_{pu}/Z_{pd} = \frac{3}{1}$ . (06 Marks)  
c. Write note on:  
(i) General logic function block.  
(ii) Multiplexer. (08 Marks)
- 7 a. Explain the design of 4-bit shifter. (10 Marks)  
b. Define regularity. Explain the design of an ALU subsystem. (10 Marks)
- 8 Write short notes on:  
a. Some general consideration in subsystem design processes.  
b. Dynamic shift register.  
c. Dynamic CMOS logic.  
d. Gray code to binary code converter. (20 Marks)

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