CBCS SCHEME

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17EE35

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define canonical minterm form and canonical maxterm form. **(05 Marks)**

b. Compare between prime implicant and essential prime implecant. Indentify all the prime implecants and essential prime implecants of the following functions using k-map :
$f(a, b, c, d) = \pi_M (0, 2, 3, 8, 9, 10, 12, 14)$. **(07 Marks)**

c. Simplify the following boolean function using k-map, and implement by logic gates.
$f(A, B, C, D, E) = \sum_m (3, 7, 10, 11, 12, 13, 14, 15, 17, 19, 21, 23, 25, 27, 28, 29, 31) + \sum_d (2, 6, 26, 30)$ **(08 Marks)**

OR

2 a. Convert the given boolean function into minterm canonical form.
$f(a, b, c) = (\bar{a} + b)(b + \bar{c})$. **(05 Marks)**

b. Simplify the following boolean fucntion using k-map
$f(P, Q, R, S) = \sum_m (0, 2, 4, 5, 6, 8, 10, 15) + \sum_d (7, 13, 14)$. **(07 Marks)**

c. Using Quine – McCluskey method, obtain a minimal SOP expression for
$f(a, b, c, d) = \sum_m (2, 3, 4, 5, 13, 15) + \sum_d (8, 9, 10, 11)$. **(08 Marks)**

Module-2

3 a. Design two bit magnitude comparator and draw the logic diagram. **(10 Marks)**

b. Write a short note on encoders. **(05 Marks)**

c. Design full adder using two numbers of 4:1 MUX. **(05 Marks)**

OR

4 a. Explain look ahead carry adder. **(10 Marks)**

b. Implement following multiple output function using IC74138 and external gates. **(05 Marks)**
$F_1 (A, B, C) = \sum_m (1, 4, 5, 7)$ and $F_2 (A, B, C) = \pi_m (2, 3, 6, 7)$.

c. Design 16:1 multiplexer using 8:1 MUX. **(05 Marks)**

Module-3

5 a. Explain the working of master slave JK flip-flops with functional table and timing diagram. Show how race around condition is overcome. **(08 Marks)**

b. Obtain characteristic equation of SR flip-flop. **(05 Marks)**

c. Explain working of 3-bit binary ripple counter with the suitable logic and timing diagram. **(07 Marks)**

OR

6 a. Convert JK flip-flop to D flip flop. **(05 Marks)**

b. Explain the 4 modes of operation of shift register with suitable logic diagram and truth table. **(08 Marks)**

c. Design MOD – 6 synchronous counter using D flip-flop. **(07 Marks)**

Module-4

7 a. Analyze the following sequential circuit given in Fig Q7(a) and obtain excitation, transition and state table. Also write the state diagram.

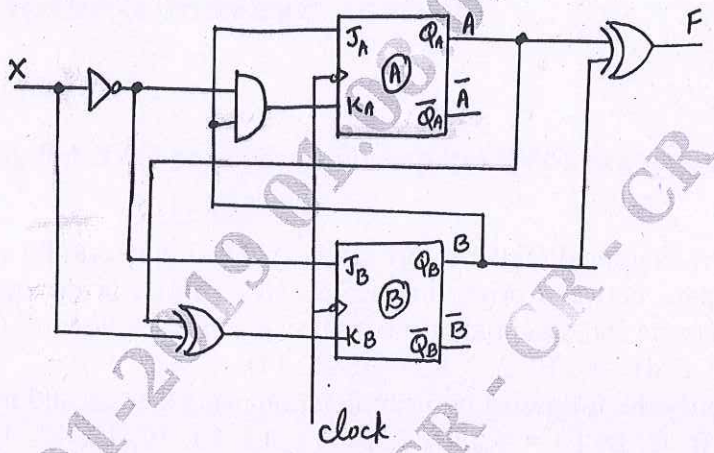

Fig Q7(a) **(12 Marks)**

b. Design a synchronous counter with the sequence 0, 1, 3, 7, 6, 4, 0 . . . . . using JK flip-flop. **(08 Marks)**

OR

8 a. Design a clocked sequential circuit that operates according to the state diagram shown in Fig Q8 (a) implement the circuit using D flip flop.

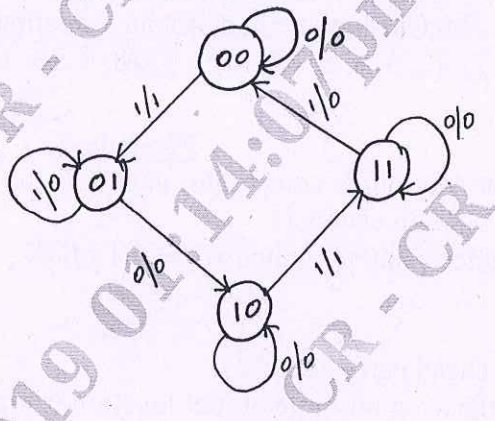

Fig Q8(a) **(12 Marks)**

b. With the help of block diagram explain Mealy and Moore model in a sequential circuit analysis. Give the example circuits. **(08 Marks)**

Module-5

9 a. Write the comparison between VHDL and verilog. **(08 Marks)**

b. Explain the various data types available in VHDL. **(06 Marks)**

c. Write HDL code of a 2 × 1 multiplexer – VHDL. **(06 Marks)**

OR

10 a. Write a data flow description for a full adder with active high enable in both VHDL and verilog. **(08 Marks)**

b. Explain shift and rotate operators in HDL with an example. **(08 Marks)**

c. Explain the structure of verilog module. **(04 Marks)**

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