CBCS SCHEME

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15EE35

Third Semester B.E. Degree Examination, June/July 2019
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Prove the following using Boolean theorems : **(04 Marks)**
i) $(x + \bar{x}\bar{y})(\bar{x}+\bar{y}) + yz = \bar{y}+z$ ii) $\bar{w}\bar{y}\bar{z} + wz + \bar{y}z + xyz = \bar{w}\bar{y} + wz + xz$.

b. Using K – maps determine all the minimal sums and products of the following Boolean function.
i) $f(w, x, y, z) = \pi m(1, 3, 4, 5, 10, 11, 12, 14)$
ii) $g(a, b, c, d) = \Sigma m(0, 1, 4, 8, 9, 10) + dc(2, 11)$. **(07 Marks)**

c. Using MEV method determine minimal sum for the following function where x, y, z are map variables. Realize the expression using double rail logic. **(05 Marks)**
$f(A, B, x, y, z) = A\bar{x}\bar{y}\bar{z} + A\bar{x}\bar{y}z + A x \bar{y} z + B\bar{x}\bar{y}z + B\bar{x} y \bar{z} + \bar{x} y z + x \bar{y}\bar{z}$.

OR

2 a. For the following Boolean function use Quine Mc Cluskey algorithm method and Petrick's method to obtain all the irredudant disjunctive normal expressions. Which of these from minimal sums? $f(a, b, c, d) = \Sigma m(0, 4, 7, 8, 11, 12, 14, 15)$. **(08 Marks)**

b. For the following function use decimal Quine Mc Cluskey method and prime implicant table reduction technique to obtain minimal sum.
$f(a, b, c, d) = \Sigma m(0, 1, 2, 4, 6, 7, 9, 11, 12, 13, 15)$. **(08 Marks)**

Module-2

3 a. Implement the following functions using IC 74139 , a – 2 to 4 decoder.
i) $f_1(abc) = \Sigma(3, 5, 6, 7)$ ii) $f_2(a, b, c) = \Sigma(1, 2, 4)$ **(04 Marks)**

b. Design a 4 to 2 line priority encoder with 'valid' output where highest priority is given to input with highest index and obtain the minimal sum expressions for outputs. Realize the expressions with basic gates. **(06 Marks)**

c. Design and implement half adder and half subtractor circuits, with a and b as inputs. **(06 Marks)**

OR

4 a. Implement $f(a, b, c) = \Sigma m(1, 4, 5, 6, 7)$ using
i) 4 – 1 MUX with 'b' and 'c' to select line ii) ii) 2 – 1 MUX with 'a' to select line
Show with K – maps and logic circuits. **(08 Marks)**

b. The 1-bit comparator had 3 outputs corresponding to a > b, a = b and a < b. It is possible to code these three outputs using two bits pq such that pq = 10 for a > b, pq = 00 for a = b and pq = 01 for a < b. This reduces the number of output lines of each 1-bit comparator to 2. The 1-bit comparator at the most significant position, however, should have a converter to convert back to three outputs. Design such a 1-bit comparator as well as the output converter network. **(08 Marks)**

Module-3

5 a. Design a switch debouncer using SR latch. Show relevant logic diagram and timing diagrams. **(06 Marks)**

b. What are characteristic equations? Derive them for SR, JK and T flip-flops. **(06 Marks)**

c. Clearly distinguish between:
i) Synchronous and asynchronous circuits
ii) Combinational and sequential circuits. **(04 Marks)**

OR

6 a. Explain with suitable logic and timing diagram:
i) Serial-in-serial out shift register
ii) Parallel-in-parallel out unidirectional shift register. **(08 Marks)**

b. Consider the synchronous counter shown in Fig.Q.6(b). Assuming it is initialized to "000" prior to the first count pulse, determine the counting sequence. Is this counter self correcting. **(08 Marks)**

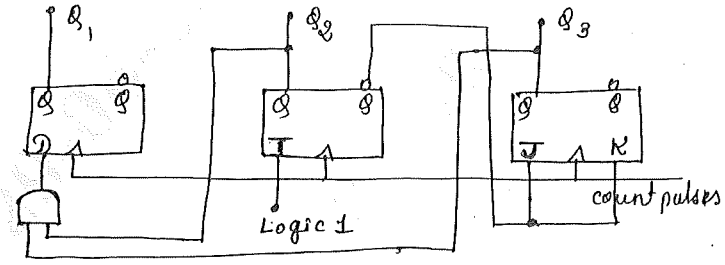

Fig.Q6(b)

Module-4

7 a. Briefly explain structure of clocked synchronous sequential network. **(05 Marks)**

b. Compare Mealy and Moore models. **(05 Marks)**

c. Construct the state table for the following state diagram in Fig.Q7(c). **(06 Marks)**

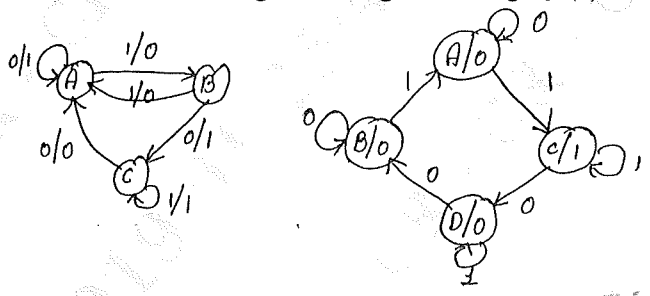

Fig.Q7(c)

OR

8 a. Design a clocked sequential circuit that operates according to state diagram shown in Fig.Q8(a). Implement the circuit using D-flip-flops. **(08 Marks)**

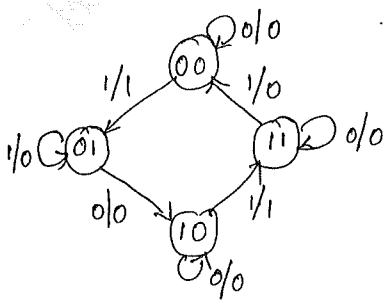

Fig.Q8(a)

b. For the clocked synchronous sequential network shown in Fig.Q8(b). Construct excitation table, transition table, state table and state diagram. **(08 Marks)**

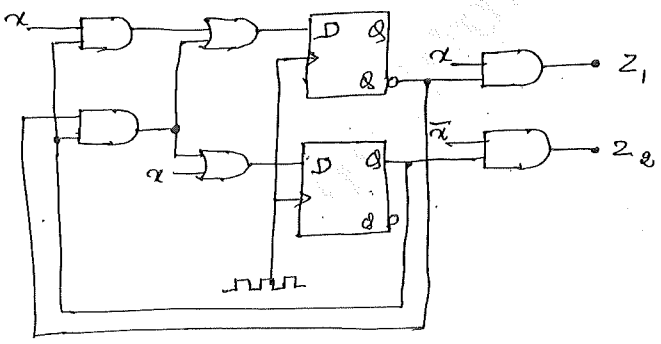

Fig.Q8(b)

Module-5

9 a. With schematic explain VHDL logical and relational operators. **(08 Marks)**

b. Briefly explain all VHDL data types. **(08 Marks)**

OR

10 a. Compare VHDL and verilog in detail. **(08 Marks)**

b. Write data flow description of a half adder (in both VHDL and verilog). Draw the truth table and derive the Boolean expressions, simulate and verify the circuit. **(08 Marks)**

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