CBCS SCHEME

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15EE46

Fourth Semester B.E. Degree Examination, June/July 2019
Operational Amplifiers and Linear IC's

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Design a capacitor coupled inverting amplifier for lower cut-off frequency (f_L) of 10Hz, voltage gain of 50, output voltage of 2.5V using 741 op-amp. **(05 Marks)**

b. Consider an amplifier circuit using op-amp with voltage series feedback. Derive an expression for the exact closed loop gain and input impedance of the circuit with feedback. **(06 Marks)**

c. With a circuit of 3-input summing amplifier in inverting mode, derive an expression for output interms of input voltages. Indicate under which condition, circuit can be used as averaging circuit. **(05 Marks)**

OR

2 a. Write a single stage amplifier using differential configuration with 4-inputs (V_1, V_2, V_3, V_4) to obtain an output $V_0 = (-V_1 - V_2 + V_3 + V_4)$. Derive the above equation. **(04 Marks)**

b. With a neat circuit, explain instrumentation amplifier (with 3-op-amps) using transducer bridge to detect change in temperature. **(06 Marks)**

c. Write a neat circuit of capacitor coupled high Z_{in} voltage follower. Obtain the expression for input impedance of the circuit and write design equations. **(06 Marks)**

Module-2

3 a. With a circuit and frequency response curve, explain I order high pass filter. Derive an expression for the gain. **(06 Marks)**

b. Explain the operation of adjustable voltage regulator using LM317 regulator. With the help of block diagram. **(05 Marks)**

c. Design a voltage follower type regulator circuit using 741 op-amp and Zener of 12V with I_z = 25mA to meet the following : i) Output voltage 12V ii) Maximum load current = 50mA. **(05 Marks)**

OR

4 a. With a circuit and frequency response curve, explain multistage wide band reject filter using highpass, lowpass and summing amplifier. Design the same to have f_1 = 400Hz and f_2 = 2KHz and passband gain of 2. **(09 Marks)**

b. Explain with a neat circuit, adjustable output regulator using voltage follower. **(07 Marks)**

Module-3

5 a. With circuit and waveforms, explain square wave/triangular wave signal generator. **(06 Marks)**

b. With circuit and waveforms, explain how Barkhausen criterion is met in RC phase shift oscillator. Design the same using ± 12V supply, for an output frequency of 3.5KHz using 741 op-amp. **(06 Marks)**

c. Write the circuit of voltage of current converter with grounded load. Derive an expression for output current. **(04 Marks)**

OR

6 a. With a circuit, explain how signal generator outputs (amplitude and DC levels) are controlled. **(04 Marks)**

b. Design an inverting Schmitt trigger for LTP = 0 V and UTP = +3V. Using 741 with $|V_{osat}|$ = 12V. Write transfer characteristics and output wave form for an input signal of 10 cos ωt. **(07 Marks)**

c. Explain with a circuit, non inverting Schmitt trigger to obtain different LTP and UTP values Write the transfer characteristics. **(05 Marks)**

Module-4

7 a. With circuit and relevant waveforms, explain full wave precision rectifier (using half wave rectifier and summing circuit). Derive an expression for output voltage showing full wave rectification. **(07 Marks)**

b. With the help of circuit and waveform, explain negative precision clamping circuit. **(04 Marks)**

c. Explain 3-bit R/2R ladder type DAC with circuit. **(05 Marks)**

OR

8 a. Briefly explain with circuit, voltage follower type positive peak detector. Design the same to be suitable for a pulsed input of 2.5V peak and 5μs rise time. Peak value is to be held for 100μs with maximum error of 1%. Also determine $I_{0(max)}$. Use BIFET op-amp. **(06 Marks)**

b. With the help of block diagram, explain successive approximation ADC. **(05 Marks)**

c. With the help of block diagram and waveform, explain dual slope ADC. **(05 Marks)**

Module-5

9 a. Explain the operation of PLL with block diagram. Briefly explain function of each component part. **(06 Marks)**

b. Briefly explain any two applications of PLL together with block diagram. **(06 Marks)**

c. Mention the features of IC555Timer. **(04 Marks)**

OR

10 a. Write the pin diagram and block diagram of IC565PLL. **(04 Marks)**

b. With circuit and waveform, explain how 555 Timer can be used as monostable multi-vibrator. **(06 Marks)**

c. Derive an expression for duty cycle of astable multi-vibrator with the help of waveforms. Mention the applications of astable multi-vibrator. **(06 Marks)**

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