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10EE764

Seventh Semester B.E. Degree Examination, June/July 2019

VLSI Circuits and Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With a neat diagram, explain the working of basic nMOS enhancement mode transistor. **(08 Marks)**

b. Explain with neat diagrams the process of fabrication of p-well CMOS inverter. **(08 Marks)**

c. Explain the procedure used for production of e-beam mask. **(04 Marks)**

2 a. Derive an expression for pull-up to pull down ratio for an nMOS inverter driven through one or more transistors and hence find the typical value for it. **(08 Marks)**

b. Explain latch-up in CMOS circuits with relevant diagrams and waveforms. **(07 Marks)**

c. An nMOS transistor has L = 2 μm, W = 20 μm and $\mu_n C_o$ = 90 μA/V^2, V_{tn} = 0.5 V. Determine drain to source current for V_{gs} = 3.3 V, V_{ds} = 2V. **(05 Marks)**

3 a. Explain Lambda (λ) based design rules as applicable to wires and transistors with appropriate diagrams. **(08 Marks)**

b. Draw the circuit symbol and stick diagrams for CMOS inverter. **(06 Marks)**

c. Draw the stick diagram and layout for nMOs shift register cell. **(06 Marks)**

4 a. What is sheet resistance? Calculate sheet resistance of transistor channel if L = 8λ, W = 2λ, if n-transistor channel $R_s = 10^4$ Ω/square. **(04 Marks)**

b. With schematic diagrams, explain inverting and non-inverting super buffers. **(06 Marks)**

c. Explain three different kinds of wiring capacitances. **(05 Marks)**

d. Briefly explain BiCMOS drivers. **(05 Marks)**

PART – B

5 a. Derive scaling factor for any 10 device parameters. **(10 Marks)**

b. Discuss the limitations of scaling on interconnect and contact resistance. **(10 Marks)**

6 a. Draw the symbolic diagram for BiCMOS 2 input NAND gate. **(06 Marks)**

b. Explain in detail pseudo nMOS logic taking inverter as an example. **(06 Marks)**

c. With block diagram and stick diagram explain the design approach of a parity generator. **(08 Marks)**

7 a. Draw and explain combinational circuit to generate 2-phase clocking. **(06 Marks)**

b. Explain pre-charged bus concept with circuit diagrams. **(06 Marks)**

c. Explain the operation of 4 × 4 cross bar switch with a neat diagram. **(08 Marks)**

8 a. Explain with diagrams and expressions how to implement ALU functions with an adder? **(10 Marks)**

b. Draw the structure of multiplexer based adder logic with stored and buffered sum output with n switches. **(10 Marks)**

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