CBCS Scheme

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15EC32

Third Semester B.E. Degree Examination, Dec.2017/Jan.2018
Analog Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive the expression for input impedance, output impedance and voltage given for common emitter fixed bias configuration using re model. **(08 Marks)**

b. Draw the graphical symbol and hybrid equivalent model for CE and CB configuration. **(04 Marks)**

c. Calculate DC bias voltage and currents for the Darlington configuration shown in Fig.Q1(c). **(04 Marks)**

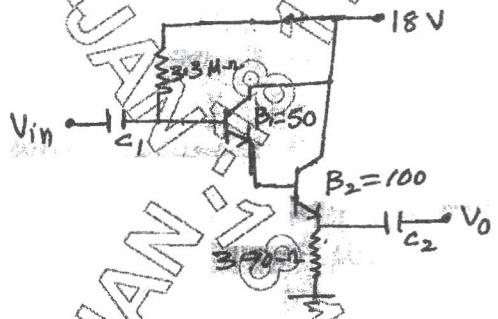

Fig.Q1(c)

OR

2 a. Derive the expression for Z_i, Z_0 and A_V for emitter–follower configuration using re-model. **(08 Marks)**

b. For the network shown in Fig.Q2(b), determine Z_i, Z_0, A_V and A_i **(08 Marks)**

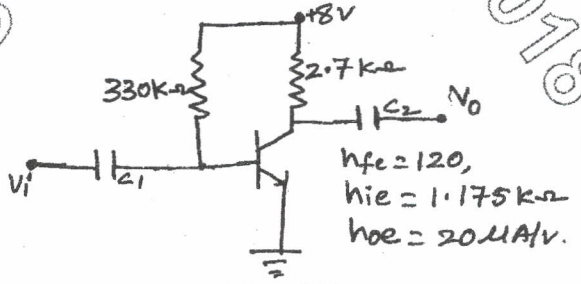

Fig.Q2(b)

Module-2

3 a. Explain the construction and working principle of n-channel JFET and draw the characteristics. **(06 Marks)**

b. Derive an expression for Z_i, Z_0 and A_V of FET self bias configuration with bypassed R_S. **(06 Marks)**

c. Distinguish between depletion type and enhancement type MOSFET. **(04 Marks)**

OR

4 a. Explain the construction and working principle of n-channel depletion type MOSFET and draw the characteristics curve. **(08 Marks)**

b. The source follower circuit shown in Fig,Q4(b) results in $V_{GSQ} = -2.86V$ and $I_{DQ} = 4.56mA$:

i) Determine g_m

ii) Determine Z_i and Z_0

iii) Determine A_v with r_d and without r_d

$I_{DSS} = 16mA$; $V_p = -4V$; $r_d = 40k\Omega$; $g_{OS} = 25\mu S$. **(08 Marks)**

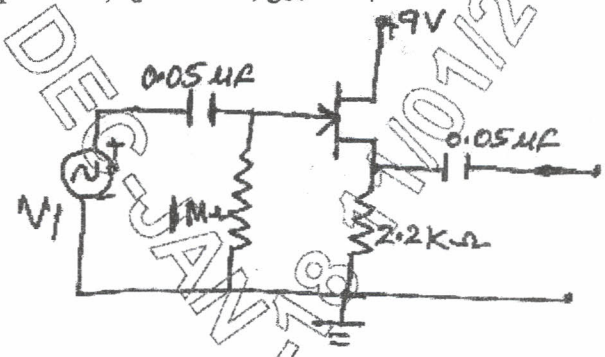

Fig.Q4(b)

Module-3

5 a. Derive the expression for low frequency response of BJT amplifier due to capacitors C_S and C_C. **(08 Marks)**

b. Calculate f_{Hi} and f_{Ho} for amplifier circuit shown in Fig.Q5(b), for the base current $I_B = 14.79\mu A$ and $A_{Vmid} = -102.58$; $\beta = 100$; $C_{be} = 20pF$; $C_{bc} = 4pF$; $h_{ie} = 1100$; $C_{wi} = 6pF$; $C_{wo} = 8pF$; $C_{CE} = 1pF$. **(08 Marks)**

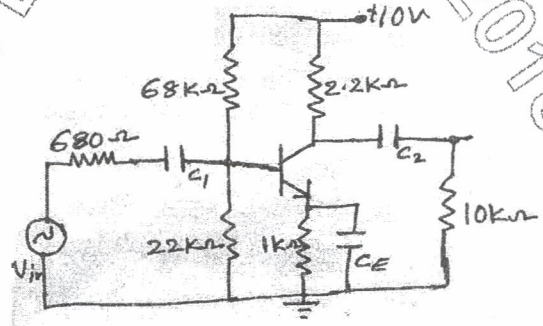

Fig.Q5(b)

OR

6 a. Derive the expression for Miller's input and output capacitance. **(08 Marks)**

b. Obtain the expression for over all lower and higher cut-off frequency for a multistage amplifier. **(08 Marks)**

Module-4

7 a. What are the advantages of negative feedback in amplifier? **(04 Marks)**

b. Derive the expression for Z_{if} and Z_{of} for voltage series feedback connection type. **(06 Marks)**

c. In a transistor Hartley oscillator, the two inductances are 2mH and 20μH while the frequency is to be changed from 950KHz to 2050KHz. Calculate the range over which the capacitor is to be varied. **(06 Marks)**

OR

8 a. Draw the circuit diagram of uni-junction oscillator and explain the principle of operation and draw the characteristics curve. **(06 Marks)**

b. With a neat circuit diagram, explain the working of colpitts oscillator using transistor. **(06 Marks)**

c. A crystal L = 0.4H, C = 0.085PF and C_m = 1PF with R = 5KΩ find :

i) Series resonate frequency

ii) Parallel resonate frequency. **(04 Marks)**

Module-5

9 a. With circuit diagram, explain the operation of transformer coupled class –A power amplifier and show that maximum efficiency is 50%. **(06 Marks)**

b. Calculate the harmonic distortion components for an output signal having a fundamental amplitude of 2.5V, second harmonic amplitude of 0.25V, third harmonic amplitude of 0.1V and fourth harmonic amplitude of 0.05V. Also calculate the total harmonic distortion. **(04 Marks)**

c. Define voltage regulator. Explain series voltage regulator using transistor. **(06 Marks)**

OR

10 a. Explain the operation of a class–B push-pull amplifier and show that maximum conversion efficiency is 78.5%. **(08 Marks)**

b. Explain shunt voltage regulator using transistor, and also find the regulated voltage and circuit currents for the shunt regulator shown in Fig.Q10(b). **(08 Marks)**

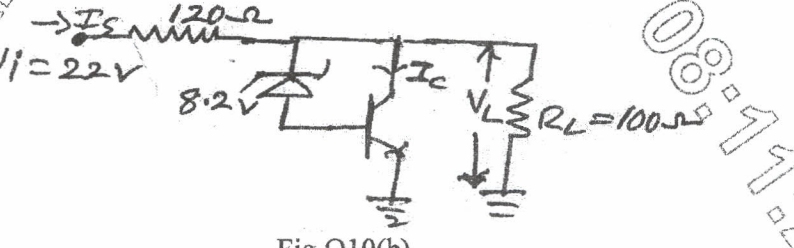

Fig.Q10(b)

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