CBCS SCHEME

USN | | | | | | | | | | 15EC53

Fifth Semester B.E. Degree Examination, Dec.2017/Jan.2018
Verilog HDL

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Explain a typical design flow for designing VLSI IC circuit using the block diagram. **(06 Marks)**

b. Explain top down design methodology and bottom up design methodology. **(10 Marks)**

OR

2 a. With a block diagram of 4-bit Ripple carry counter, explain the design hierarchy. **(10 Marks)**

b. Explain the trends in Hardware Description Languages (HDLs). **(06 Marks)**

Module-2

3 a. With a neat block diagram, explain the components of verilog module. **(06 Marks)**

b. Explain the following data types with an example in verilog:
(i) Nets (ii) Register (iii) Integers (iv) Real (v) Time Register. **(10 Marks)**

OR

4 a. Explain the port connection rules. **(06 Marks)**

b. Explain the two methods of connecting ports to external signals with an example. **(10 Marks)**

Module-3

5 a. What are Rise, Fall and Turn-off delays? How they are specified in verilog? **(06 Marks)**

b. Design a 2-to-1 multiplexer using bufifo and bufifl gates. The delay specification for these gates are as follows:

Delay	Min	Typ	Max
Rise	1	2	3
Fall	3	4	5
Turn-off	5	6	7

Write gate level description and stimulus in verilog. **(10 Marks)**

OR

6 a. Write a verilog dataflow level of abstraction for 4-to-1 multiplexer using conditional operator. **(06 Marks)**

b. Write a verilog dataflow description for 4-bit Full adder with carry lookahead. **(10 Marks)**

Module-4

7 a. Explain the blocking assignment statements and non-blocking assignment statements with relevant examples. **(08 Marks)**

b. Write a note on the following loop statements:
(i) While loop (ii) forever loop. **(08 Marks)**

OR

8 a. Explain sequential and parallel blocks with examples. **(08 Marks)**

b. Write a verilog program for 8-to-1 multiplexer using case statement. **(08 Marks)**

Module-5

9 a. Explain the synthesis process with a block diagram. **(08 Marks)**

b. Write a VHDL program for two 4-bit comparator using data flow description. **(08 Marks)**

OR

10 a. Explain the declaration of constant, variable and signal in VHDL with example. **(08 Marks)**

b. Write a VHDL program for half adder in behavioral description. **(08 Marks)**

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