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10EC751

Seventh Semester B.E. Degree Examination, Dec.2017/Jan.2018
DSP Algorithms and Architecture

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting
atleast TWO questions from each part.**

PART – A

- 1 a. With the help of block diagram and equations explain decimation and interpolation process. Also determine the interpolated sequence $y(m)$, if the signal sequence $x(n) = \{0, 2, 4, 6, 8\}$ is interpolated using the interpolation filter sequence $b_k = [0.5, 1, 0.5]$. Interpolation factor $L = 2$. (10 Marks)
- b. Explain with the block diagram of a DSP system. Also draw the typical signals in a DSP scheme. (08 Marks)
- c. Assuming $x(k)$ as a complex sequence, determine the number of complex and real multiplies for computing DFT, using direct and radix – 2 FFT algorithms. assume $N = 1024$. (02 Marks)
- 2 a. Mention the basic features that should be provided in the DSP architecture to be used to implement the following N^{th} order FIR filter $y(n) = \sum_{i=0}^{N-1} h(i)x(n-i)$; $n = 0, 1, 2, \dots$. (04 Marks)
- b. Explain the register pointer updating algorithm for circular buffer. (06 Marks)
- c. With relevant block diagram, explain the various features of arithmetic and logic unit of DSP processor. (06 Marks)
- d. Write a note on organization of the on-chip memory. (04 Marks)
- 3 a. Compare the architectural features of TMS320C25 and DSP56000. (08 Marks)
- b. Draw the functional diagram of the barrel shifter of TMS320C54XX processor and explain the significance of each block. (08 Marks)
- c. Assuming the current contents of AR3 to be 200h, what will be its contents after each of the following TMS320C54XX addressing modes is used. Assume that the contents of ARO are 40h i) *AR3 – 0 ii) *AR3 + iii) **AR3(50h) iv) *AR3 – OB. (04 Marks)
- 4 a. Explain the pipeline operation of TMS320C54XX processor. Show the pipeline operation of the following sequence of instructions if the initial value of AR3 is 85h and the values stored in memory location 85h, 86h, 87h are 5, 6 and 7.
LD *AR3 +, A
ADD # 1000h, A
STL A, *AR3 +. (08 Marks)
- b. Write the TCR register format and explain the functions of the various bits in the TCR register. (06 Marks)
- c. Write a program to compute the sum of three product terms given by the equation :
 $y(n) = h_0x(n) + h_1x(n-1) + h_2x(n-2)$ where $x(n)$, $x(n-1)$, $x(n-2)$ are data samples stored at three successive data memory locations h_0 , h_1 , h_2 are constants stored in data memory. Use direct addressing mode. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – B

- 5 a. Represent each of the following as 16 – bit numbers in the desired Q – notation :
- 0.3125 as a Q_{15} number
 - 0.3125 as a Q_{15} number
 - 3.125 as a Q_7 number
 - 352 as a Q_0 number. (04 Marks)
- b. Write a TMS320C54XX program for the implementation of an interpolating FIR filter of length 15 and interpolating factor 5. (08 Marks)
- c. Write a program to multiply two Q_{15} numbers in TMS320C54XX processor. (04 Marks)
- d. Briefly explain IIR filters. With the help of block diagram, explain second order IIR filters. (04 Marks)
- 6 a. Determine the following for a 128 – point FFT computations :
- Number of stages
 - Number of butterflies in each stage
 - Number of butterflies needed for the entire computation
 - Number of butterflies that need no twiddle factor. (04 Marks)
- b. Write subroutine for bit reverse address generation and explain the same. (06 Marks)
- c. Explain the butterfly computation in DIT FFT algorithm and write a subroutine that implements the butterfly computation. (10 Marks)
- 7 a. Draw the timing diagram of the memory interface signals for a read – read –write sequence of operations. Also explain the purpose of each signal. (06 Marks)
- b. Explain the register sub-addressing technique for configuring DMA. (04 Marks)
- c. Interface the TMS320C54XX to a 10 –bit ADC(TLC1550) and an 8 bit DAC (TLC7524). The sampled signal read from the ADC is to be written to the DAC after adjusting its size. The start of conversion is initiated by the TOUT signal. Write a flowchart for main program and interrupt service routine and also write the program. (10 Marks)
- 8 a. With a neat block diagram and timing diagram for transmit and receive operation, explain the signals involved in synchronous serial interface. (08 Marks)
- b. With the help of block diagram, explain DSP based biotelemetry receiver system. (06 Marks)
- c. Explain the image compression and reconstruction using JPEG encoder and decoder. (06 Marks)
