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10TE74

Seventh Semester B.E. Degree Examination, Dec.2017/Jan.2018
DSP Algorithm and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain with block diagram a DSP system, Also draw the typical signals in a DSP system. **(08 Marks)**

b. Implement an IIR filter whose output is obtained by taking 90% of past output and 10% of current input. Plot magnitude and phase response. **(06 Marks)**

c. Determine the interpolated sequence y(m), if the signal sequence x(n), is interpolated using the interpolation filter sequence b_k. x(n) = {0, 2, 4, 6, 8} $b_k = \left\{\frac{1}{2}, 1, \frac{1}{2}\right\}$ and interpolation fator L = 2. **(06 Marks)**

2 a. Mention the basic architectural features that should be provided by a programmable DSP device. **(06 Marks)**

b. What is the significance of shifter in DSP architecture? Explain the implementation of a 4 bit, shift-right barrel shifter. **(08 Marks)**

c. With relevant Block diagram, explain Address generation unit. **(06 Marks)**

3 a. Draw the functional diagram of the multiplier/adder unit of TMS320C54XX processors and explain its salient features. **(06 Marks)**

b. Write a note on program control. **(06 Marks)**

c. Assuming the current contents of AR3 to be 200h, what will its content be after each of the following: TMS320C54×× addressing modes in used?
Assume AR0 = 40h.
i) *AR3 – 0 ii) *AR3+ iii) *AR3 iv) *+AR3 (50h)
v) *AR3 + 0% vi) *AR3 – 0B viii) *AR3 + 0B viii) *AR3 + 0. **(08 Marks)**

4 a. Write a program to find the sum of a series of signed numbers stored at successive memory locations in the data memory and place the result in A-register $A = \sum_{i=41oh}^{4Ifh} D \bmod (i)$ **(06 Marks)**

b. Draw the logical block diagram of timer circuit and explain its operation. **(06 Marks)**

c. Explain the pipeline operation TMS320C54XX processor, show the pipeline operation of the following sequence of instructions if the initial value of AR3 is 85h and the values stored in memory location 85h, 86h, 87h are 5, 6 and 7 respectively
LD *AR3+, A
ADD #1000h, A
STL A, * AR3+ **(08 Marks)**

PART – B

5 a. Represent each of the following as 16 bit numbers in the desired Q- notation.
   i) 0.3125 as a Q_{15} number
   ii) –0.3125 as a Q_{15} number
   iii) 3.125 as Q_7 number
   iv) –352 as a Q_0 number. **(04 Marks)**

   b. Write an assembly language program for TMS320C54XX processor to implement an FIR filter. **(10 Marks)**

   c. Write a program for implementation of the decimation filter for TMS320C54XX processor. **(06 Marks)**

6 a. Explain how bit reversed index generation can be done in an 8-point DFT computation and Also write on subroutine for bit reverse address generation. **(08 Marks)**

   b. Determine the following for a 256 point FFT computation.
   i) Number of stages
   ii) Number of butterflies in each stage
   iii) Number of butterflies needed for the entire computation
   iv) Number of butterflies that need no twiddle factor. **(04 Marks)**

   c. Explain the concept of overflow and scaling during butterfly computation. **(08 Marks)**

7 a. Design a data memory system with address range from 000800h – 000fffh for a C5416 processor. Use 2K × 8 SRAM memory chips. **(06 Marks)**

   b. Draw the timing diagram of the I/O interface signals for a read – write – read sequence of operations. **(05 Marks)**

   c. Interface the TMS320C54XX to a 10 bit ADC (TLC1550) and an 8 bit DAC(TLC7524). The sampled signal read from the ADC is to be written to the DAC after adjusting its size. Write the flow charts for main program and ISR. Also write the program. **(09 Marks)**

8 a. With a neat block diagram and timing diagram for transmit and receive operation, explain the signals involved in synchronous serial interface. **(08 Marks)**

   b. With the help of block diagram, explain DSP based biotelemetry receiver system. **(06 Marks)**

   c. Explain the image compression and reconstruction using JPEG encoder and decoder. **(06 Marks)**

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