ONE TIME EXIT SCHEME

USN | | | | | | | | | |

10EC56

Fifth Semester B.E. Degree Examination, April 2018
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain how transistor works in enhancement mode for the values of V_{ds} , V_{gs} and V_t . **(08 Marks)**

b. With a neat diagram explain n-MOS fabrication process. **(08 Marks)**

c. What are transmission gates? Give an example for circuit using transmission gates. **(04 Marks)**

2 a. What do you mean by Lambda (λ) based design rule and write the design rules for wires of n-MOS and CMOS and transistors. **(10 Marks)**

b. Using CMOS configuration, draw a neat schematic and stick diagram for the following :

(i) $Y = \overline{a + b \cdot c}$ ii) $f = \overline{x \cdot y + z \cdot w}$ **(10 Marks)**

3 a. Describe the dynamic CMOS logic using CMOS NOR gate for 2 inputs. **(08 Marks)**

b. With an example of CMOS NAND gate, explain CMOS Domino logic. **(08 Marks)**

c. Write note on BiCMOS logic. **(04 Marks)**

4 a. Explain the propagation delay in cascaded pass transistors. **(10 Marks)**

b. Using expressions explain scaling factors for device parameters viz: Gate area, gate capacitance per unit area, gate capacitance, parasitic capacitance and gate delay. **(10 Marks)**

PART – B

5 a. List the architectural issues of subsystem design. **(04 Marks)**

b. With a neat diagram and relevant expressions explain parity generator structural design. **(10 Marks)**

c. Describe switch logic implementation of a four-way multiplexer. **(06 Marks)**

6 a. List and explain the different stages of design process. **(06 Marks)**

b. Explain with a diagram 4×4 Barrel shifter. **(06 Marks)**

c. Describe 4-bit serial-parallel multiplier. **(08 Marks)**

7 a. Explain three transistor dynamic memory RAM cell, using CMOS circuit and stick diagram. **(10 Marks)**

b. With a neat diagram explain four transistor dynamic and six transistor static memory cell. **(10 Marks)**

8 a. Write a note on test and testability. **(10 Marks)**

b. Design and explain the floor plan for 4-bit processor. **(10 Marks)**

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