CBCS SCHEME

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15EC655

Sixth Semester B.E. Degree Examination, June/July 2018
Microelectronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive the expression for drain to source current for triode and saturation regions of n-MOSFET. **(10 Marks)**

b. Design the circuit shown in Fig.Q1(b) to obtain a drain voltage of 0.1V. Find the value of R_D. At the operating point, let $V_t = 0.5V$ and $K'_n\left(\frac{W}{L}\right) = 2mA/V^2$. **(06 Marks)**

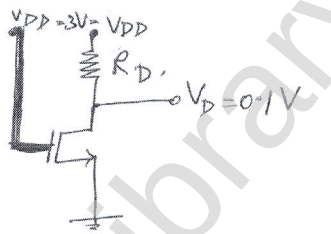

Fig.Q1(b)

OR

2 a. Derive the expression for drain current under channel length modulation. **(08 Marks)**

b. What is body effect? Write the expressions for V_t related to body effect and draw its small signal model. **(04 Marks)**

c. Design the circuit in Fig.Q2(c) to obtain $I_D = 80\ \mu A$, find the value required for R and find the DC voltage V_D. Let the NMOS transistor have $V_t = 0.6V$, $\mu_n cox = 200\ \mu A/V^2$, $L = 0.8\mu m$ and $W = 4\ \mu m$. Neglect channel length modulation. **(04 Marks)**

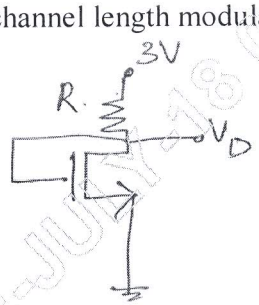

Fig.Q2(c)

Module-2

3 a. Briefly explain any two types of baising methods in MOS amplifier circuits. **(06 Marks)**

b. Derive the expression for transconductance gm and voltage gain Av for a CS amplifier with small input signal. **(10 Marks)**

OR

4 a. Develop a T equivalent model for the MOSFET from a hybrid π model. **(08 Marks)**

b. For a n-channel MOSFET with $t_{ox} = 10nm$, $L = 1.0\mu m$, $W = 10\mu m$, $L_{OV} = 0.05\mu m$, $C_{sbo} = C_{dbo} = 10fF$, $V_0 = 0.6V$, $V_{SB} = 1\ V$ and $V_{DD} = 2V$. Calculate the following capacitances when the transistor is operating in saturation C_{OX}, C_{OV}, C_{gs}, C_{gd}, C_{db}, C_{sb}. Given $E_{OX} = 3.45 \times 10^{-11}\ F/m^2$. **(08 Marks)**

Module-3

5 a. Make a comparison between BJT and MOSFET (Any 4 characteristics). **(08 Marks)**

b. Determine the G_V, A_y, R_{out}, R_{in}, A_{VO} for a common source MOS amplifier without source degeneration. **(08 Marks)**

OR

6 a. Explain the operation of a MOS current steering circuit and mention its advantage. **(08 Marks)**

b. Consider CG amplifier designed using a circuit. Given g_m = 1mA/V and R_D= 15 kΩ. Find R_{in}, R_{out}, A_V, A_{VO}, and G_V for R_L = 15kΩ and R_{sig} = 50Ω. **(08 Marks)**

Module-4

7 a. A CMOS CS amplifier fabricated in 0.18μm technology has W/L = 7.2μm/0.36μm for all transistor K_n' =387μA/V^2, K_p' = 86 μA/V^2, I_{ref} = 100μA, V_{An}' = 5V/μm and $|V_{AP}|$ = 6V/μm. Find g_{m_1}, r_{o_1}, r_{o_2} and voltage gain. **(08 Marks)**

b. For a CG amplifier with active load determine the expression for R_i, A_{VO}, A_V, G_{VO}, G_V, R_O. **(08 Marks)**

OR

8 a. Write a notes on : i) Double cascode ii) Folded cascode. **(08 Marks)**

b. Explain CMOS implementation of common source amplifier. **(08 Marks)**

Module-5

9 a. For a MOS differential pair with a common mode voltage V_{CM} is shown in Fig. Q9 (a). Let $V_{DD} = V_{SS} = 1.5V$, $K_n'\left(\frac{W}{L}\right) = 4mA/V^2$, V_t = 0.5V, I = 0.4 mA and R_D = 2.5kΩ. Neglect channel length modulation.

i) Find V_{OV} and V_{GS} for each transistor

ii) For V_{CM} = 0, find V_S, id, id_2, Vd_1 and Vd_2

iii) Repeat (b) for V_{CM} = +1V

iv) What is the highest value for which Q_1 and Q_2 are in saturation? If current I requires a minimum voltage of 0.4V to operate properly. What is the lowest allowed V_S and hence V_{CM}? **(10 Marks)**

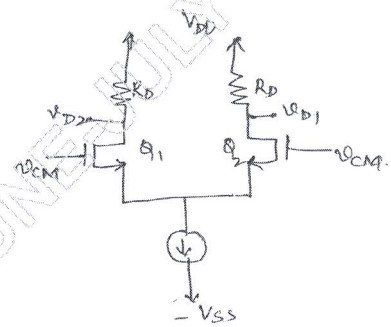

Fig.Q9(a)

b. What is the effect of mismatch of R_D on CMRR of a MOS differential amplifier? **(06 Marks)**

OR

10 a. Explain the operation of MOS differential pair with a differential input signal. **(08 Marks)**

b. Explain 2–stage CMOS OPAMP configuration. **(08 Marks)**

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