ONE TIME EXIT SCHEME

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10TE74

## Seventh Semester B.E. Degree Examination, April 2018
## DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

**Note:** ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***



### PART – A

1 a. With a neat block diagram, explain digital signal processor. Also discuss the issues to be considered in designing and implementing a DSP system. **(08 Marks)**

b. Write the block diagram representation of digital filter and compare FIR and IIR filter. **(08 Marks)**

c. Given x(n) = [1, 2, 3, 4], $b_K$[5, 6, 7, 8] and interpolation factor = 2. Find the interpolated sequence y(m). **(04 Marks)**

2 a. Classify the various types of addressing modes with an example. Also discuss the specialized addressing modes. **(12 Marks)**

b. Explain in purpose of a program sequences with a block diagram. **(08 Marks)**

3 a. With a neat diagram, explain multiplier and adder unit of TMS320C54XX DSP processor. **(08 Marks)**

b. With the help of block diagram, explain indirect addressing mode of C54XX DSP processor. **(06 Marks)**

c. Explain sequential and other types of program control. **(06 Marks)**

4 a. Describe the operation of the following instructions of C54XX processor with an example:
i) RPTB ii) MACD iii) MAS **(06 Marks)**

b. Describe the operation of hardware timer with a neat diagram. **(06 Marks)**

c. Explain the different stages of pipelining in TMS320C54XX processor. **(08 Marks)**



### PART – B

5 a. Explain how the FIR filter algorithm can be implemented using C54XX processor. **(10 Marks)**

b. Explain with the help of a block diagram and mathematic equations, the implementation of a second order IIR filter. No program code is expected. **(10 Marks)**

6 a. Derive the expression for optimum scaling factor for DIT FFT butterfly algorithm. **(06 Marks)**

b. What do you mean by bit reversed index generation? How it is implemented in C54XX DSP? **(07 Marks)**

c. Write a subroutine program to find the spectrum of the transformed data using C54XX DSP. **(07 Marks)**

7 a. Design a data memory system with address range 000800H-000FFFH for a C5416 processor. Use 2K × 8 SRAM memory chips. **(06 Marks)**

b. With a flow chart, explain how interrupts can be handled in DSP processor. **(08 Marks)**

c. Explain register sub addressing technique for configuring DMA operation. **(06 Marks)**

8 a. With the help of block diagram, explain the image compression and reconstruction using JPEG encoder and decoder. **(10 Marks)**

b. Explain DSP based encoding and decoding scheme for pulse position modulation signal. **(10 Marks)**

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