CBCS SCHEME

USN | | | | | | | | | | **15EC32**

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Analog Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Define h parameters using two port systems. **(05 Marks)**

b. Derive expressions for input impedance, output impedance and voltage gain for common emitter fixed bias configuration using re model. **(07 Marks)**

c. Find Z_i, Z_o, A_v and A_i for the network shown in Fig.Q.1(c). Given data $h_{fb} = -0.99$, $h_{ib} = 14.3\Omega$, $h_{ob} = 0.5\ \mu A/v$. **(04 Marks)**

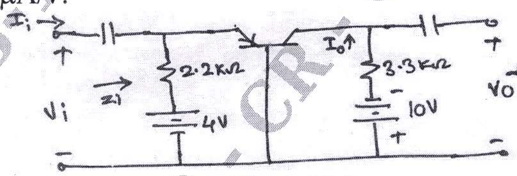

Fig.Q.1(c)

OR

2 a. Explain hybrid π model. **(04 Marks)**

b. Find r_e, Z_i, Z_o and A_v for the circuit shown in Fig.Q.2(b). Given data $B = 90$, $r_o = 50k\Omega$. **(05 Marks)**

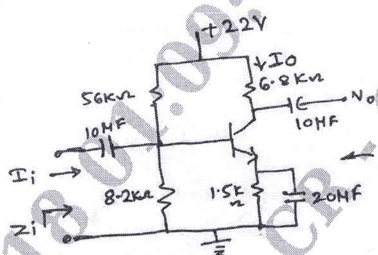

Fig.Q.2(b)

c. Derive the expressions for Z_i, Z_o, A_v and A_i for fixed bias configuration using approximate Cε hybrid equivalent model. **(07 Marks)**

Module-2

3 a. List the differences between JFET and MOSFET. **(04 Marks)**

b. Explain with neat sketches, operation and characteristics of n-channel E-MOSFET. **(08 Marks)**

c. Find: i) input impedance ii) output impedance iii) voltage gain for the circuit shown in Fig.Q.3(c). Given data $g_m = 2ms$, $r_d = 50K\Omega$. **(04 Marks)**

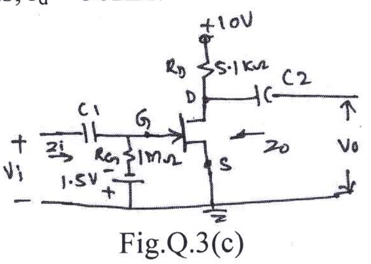

Fig.Q.3(c)

OR

4 a. Find transconductance and drain current for the JFET if I_{DSS} = 20mA, V_P = -5V, V_{GS} = -4V and gmo = 4ms. **(04 Marks)**

b. Derive an expressions for Z_i, Z_o and A_v using small signal JFET amplifier under fixed bias configuration. **(07 Marks)**

c. Sketch the following circuit diagrams:
i) JFET ac equivalent model of source follower
ii) Cascaded FET amplifier. **(05 Marks)**

Module-3

5 a. An amplifier rated at a 40W output is connected to a 10Ω speaker, Find:
i) Input power required for full output if power gain is 25dB
ii) Input voltage for rated output if the amplifier voltage gain is 40dB. **(04 Marks)**

b. Explain high frequency response of FET amplifier. **(07 Marks)**

c. Explain multistage frequency effects. **(05 Marks)**

OR

6 a. Derive an expressions for Miller input and output capacitor. **(06 Marks)**

b. Determine A_V, Z_i and A_{vs} for the law frequency response of the BJT amplier circuit shown in Fig.Q.6(b). Assume $r_0 = \infty$. **(06 Marks)**

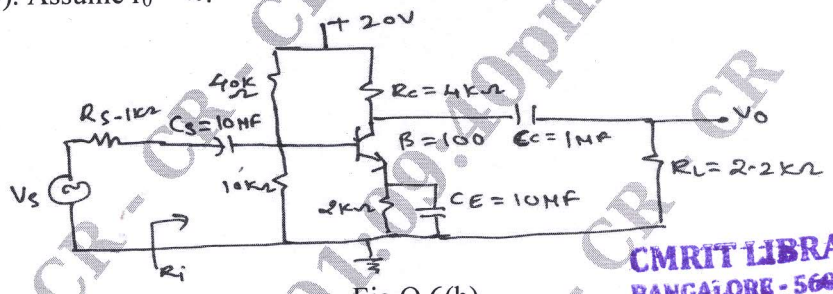

Fig.Q.6(b)

c. Draw the circuit diagram of high frequency response of BJT amplifier under CE mode with capacitances. **(04 Marks)**

Module-4

7 a. List the conditions for sustained oscillations. **(04 Marks)**

b. Determine the voltage gain, input impedance and output impedance with feedback for series voltage feedback having A = -100, R_i = 10KΩ and R_o = 20KΩ for feedback factor β = -0.1. **(05 Marks)**

c. Explain with neat circuit diagram the operation of colpit oscillator. **(07 Marks)**

OR

8 a. Show that gain with feedback in voltage series feedback system reduced by a factor (1 + AB). **(05 Marks)**

b. Explain the operation of FET RC phase oscillator with neat circuit diagram. **(06 Marks)**

c. Design the RC elements of a Wein bridge oscillator for the operation at f = 10kHz and draw the oscillator circuit diagram. **(05 Marks)**

Module-5

9 a. Define class A, class B, class C and class D power amplifiers. **(04 Marks)**

b. Calculate the output voltage and the zener current for the regulator shown in Fig.Q9(b) for $R_L = 1K\Omega$. **(04 Marks)**

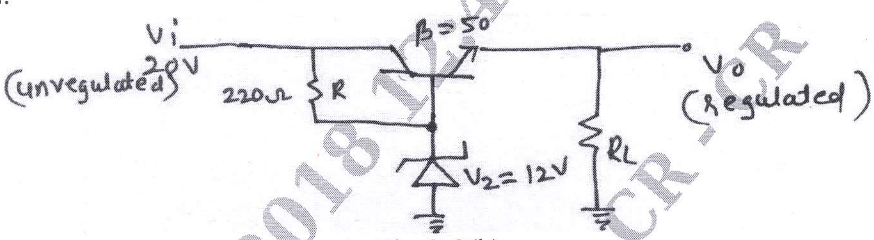

Fig.Q.9(b)

c. Explain with neat diagram and waveforms class B push pull power amplifier. **(08 Marks)**

OR

10 a. Compare the series and shunt voltage regulators. **(04 Marks)**

b. Define the following:

i) Cross over distortion
ii) Harmonic distortion
iii) Percentage load regulation
iv) Amplifiers efficiency **(04 Marks)**

c. Calculate input power, output power and efficiency of the series fed class A power amplifier circuit shown in Fig.Q10(c). **(08 Marks)**

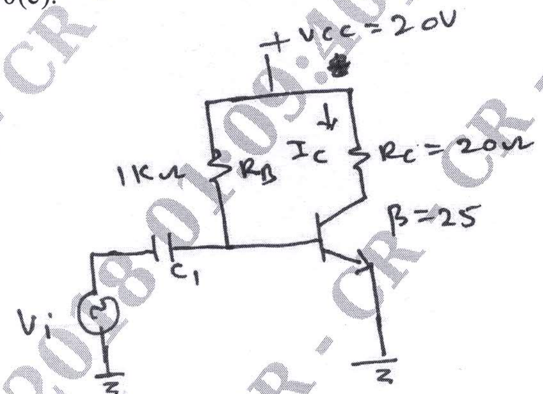

Fig.Q.10(c)

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