CBCS SCHEME

USN | | | | | | | | | | 15EC32

Third Semester B.E. Degree Examination, June/July 2019
Analog Electronics

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Derive the expression for Z_{in}, Z_0, A_v and A_I for voltage divider bias CE amplifier with R_E unbypassed using re-model. **(10 Marks)**

b. Write a note on hybrid π model. **(06 Marks)**

OR

2 a. For a emitter bias circuit with $R_B = 470k\Omega$, $R_C = 3.3\Omega$, $R_E = 1.2k\Omega$, $C_{C_1} = C_{C_2} = 0.1\mu F$, $h_{fe} = 120$, $h_{ie} = 1k\Omega$, $h_{oe} = 50\mu\mho$. Find A_I, A_V, Z_{in} and Z_0 if R_E is unbypassed. Also write the hybrid model. **(08 Marks)**

b. Derive the expression for Z_{in}, Z_0, A_V and A_I for common collector configuration amplifier using approximate hybrid model. **(08 Marks)**

Module-2

3 a. Derive the expression for transconductance also relate I_D and g_m. **(06 Marks)**

b. Obtain the expression for Z_{in} and A_V for a JFET common gate amplifier. Write the small signal model. **(10 Marks)**

OR

4 a. For a common drain configuration amplifier if $R_G = 2\mu\Omega$, $R_S = 2.2k\Omega$, $V_{DD} = 20V$, $C_{C_1} = C_{C_2} = 0.1\mu F$. Find Z_{in}, Z_0 and A_V given. $I_{DSS} = 10mA$, $V_p = -5V$, $r_d = 40k\Omega$, $V_{GSQ} = -2.85V$. **(06 Marks)**

b. With a neat diagram, explain the construction and operation of D–MOSFET and E–MOSFET. Also write the drain and transfer characteristics. **(10 Marks)**

Module-3

5 a. State Miller's theorem and also obtain the expression for input and output capacitances. **(08 Marks)**

b. Derive the expressions for low frequency response of BJT amplifier due to input and output coupling capacitors and also due to bypass capacitor. **(08 Marks)**

OR

6 a. Determine the higher frequency response of the amplifier circuit shown in Fig.Q6(a) below, also plot the graph.

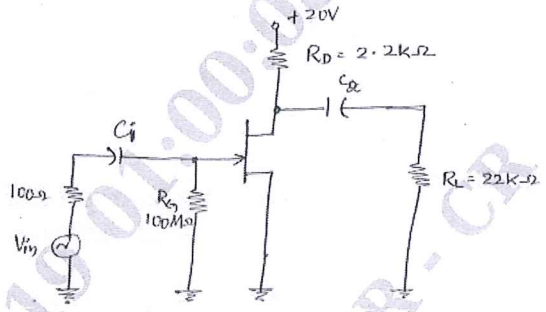

Fig.Q6(a)

b. Given $V_{GS} = -8V$, $I_{GSS} = 80mA$, $g_m = 6ms$, $C_{gs} = 4pF$, $C_{gd} = 2pF$. **(08 Marks)**
Obtain the expression for overall tower and upper cutoff frequency of multistage amplifier. **(08 Marks)**

Module-4

7 a. Prove that input and output impedances in voltage shunt feedback amplifier decreases. **(06 marks)**

b. With the help of neat block diagram, deduce the conditions for sustained oscillations. **(04 marks)**

c. Explain the important advantages of negative feedback. **(06 marks)**

OR

8 a. For a Wein bridge oscillator, if $R_i = 1k\Omega$ and $R_F = 2.5k\Omega$. Find frequency of oscillation for $R = 2k\Omega$ and $C = 10mF$. Is oscillations sustained? **(04 Marks)**

b. Derive the expression for frequency of oscillation in Hartley oscillator with the help of neat circuit diagram. **(06 Marks)**

c. Explain the construction and operation of UJT. **(06 Marks)**

Module-5

9 a. Explain push pull amplifier with a neat circuit diagram. Show that its maximum conversion efficiency is 78.5%. **(12 Marks)**

b. Write a note on class C amplifiers. **(04 Marks)**

OR

10 a. Explain services and shunt voltage regulator. **(10 marks)**

b. For the circuit shown in Fig.Q10(b) below, if peak base circuit is 1mA. Calculate :
i) $P_{0(ac)}$ ii) $P_{in(dc)}$ iii)$\eta(\%)$. **(06 Marks)**

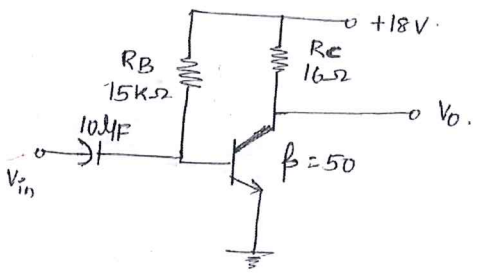

Fig.Q10(b)

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