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10EC56

**Fifth Semester B.E. Degree Examination, June/July 2019**  
**Fundamentals of CMOS VLSI**

Time: 3 hrs.

Max. Marks: 100

**Note: Answer any FIVE full questions, selecting at least TWO questions from each part.**

**PART - A**

1. a. With the help of neat diagram, explain the CMOS p-well process steps. Draw the CMOS p-well inverter. (10 Marks)
- b. Write the voltage – transfer characteristics of an CMOS inverter. Derive the relevant equation to justify the characteristics. (10 Marks)
2. a. Explain design rule check and give the Lambda based design rules for
  - i) nMOS and CMOS wire
  - ii) Contacts. (08 Marks)
- b. Draw the schematic and layout for the function  $Y = \overline{A + BC}$  in CMOS design style. (08 Marks)
- c. Draw the schematic circuit for the given layout in Fig Q2(c)

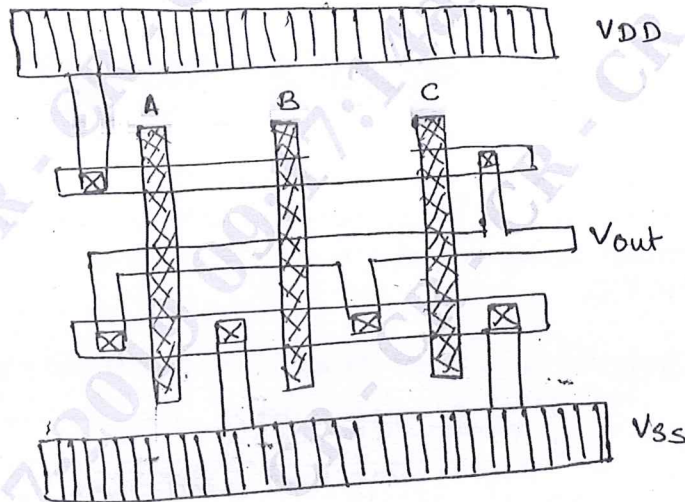


Fig Q2(c)

(04 Marks)

3. a. Cascading of dynamic CMOS logic structure leads to an erroneous evaluation. Justify. Explain how it is overcome in domino CMOS logic. Give the advantages and disadvantages of domino CMOS logic. (10 Marks)
- b. Draw the Pseudo – nMOS logic structure for the expression  $Y = \overline{(AB + DE)C}$ . (05 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

- c. Find out the node voltage and  $V_{out}$  of the given pass transistor chain shown in Fig Q3(c)-(i) and Q 3(c)-(ii) to pass logic 1.

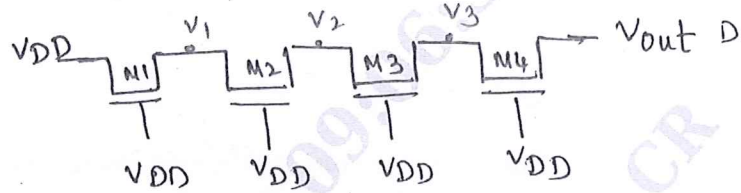


Fig Q3(c)-(i)

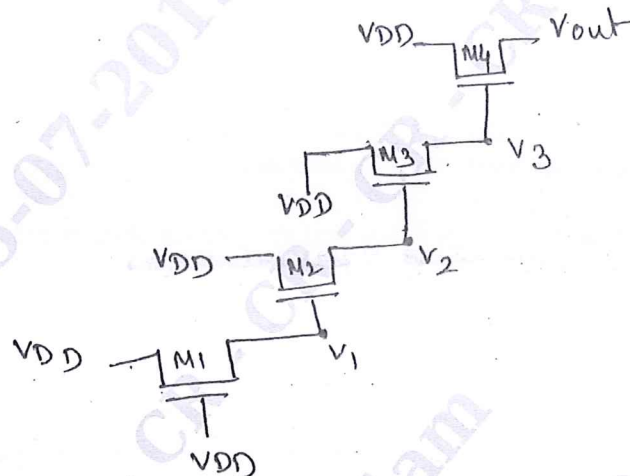


Fig Q 3(c)-(ii)

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(05 Marks)

- 4 a. Using the rise time and fall time model of CMOS inverter. Prove  $\tau_r = 2.5\tau_f$  (08 Marks)
- b. Calculate the total capacitance of the multilayered structure shown in Fig Q4(b) with gate to channel capacitance of  $1 \square C_g$ , poly to substrate of  $0.1 \square C_g$  and Metal 1 to substrate of  $0.075 \square C_g$ . (07 Marks)
- c. Obtain the scaling factor of Gate delay and power dissipation per gate. (05 Marks)

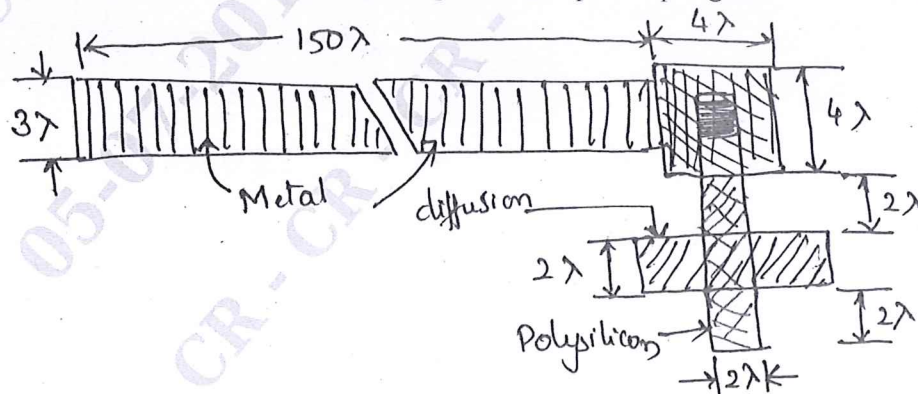


Fig Q4(b)

**PART – B**

- 5 a. Design a bus arbitration logic for n-line bus using structure design approach. (10 Marks)  
b. What is charge storage? Explain a 4-bit dynamic shift register using nMOS switch. (10 Marks)
- 6 a. List the general subsystem design consideration. (05 Marks)  
b. Define the term regularity. Explain in detail the design of 4-bit carry look ahead adder. (10 Marks)  
c. Draw the logical diagram of 4-bit Baugh-Wooley multiplier. (05 Marks)
- 7 a. Describe the operation of 3-T dynamic RAM cell. Analyse the circuit for the parameter Area, Dissipation and volatility. (10 Marks)  
b. Describe the read and write operation of 4-T dynamic and 6-T static memory cell with a neat circuit diagram. (10 Marks)
- 8 a. Explain the practical guidelines for testability to facilitate the test processes. Any five of them. (10 Marks)  
b. Explain in detail the BILBO built in test generation scheme for the normal and scan modes of operation. (10 Marks)

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