



# CBCS SCHEME

15EC53

## Fifth Semester B.E. Degree Examination, June/July 2019 Verilog HDL

Time: 3 hrs.

Max. Marks: 80

*Note: Answer any FIVE full questions, choosing ONE full question from each module.*

### Module-1

- 1 a. Discuss different type of module level with an example. (08 Marks)
- b. List the basic type of design methodology. Differentiate between them. (08 Marks)

OR

- 2 a. What do you mean by instantiation and instances? Write a verilog code for 4 bit ripple carry counter to show instantiation and instances. (08 Marks)
- b. What is the need of stimulus block in simulation, discuss with an example. (08 Marks)

### Module-2

- 3 a. List and explain different system tasks and compiler directives of verilog. (10 Marks)
- b. List the components of a verilog module. Write a verilog code to list the components of SR latch. (06 Marks)

OR

- 4 a. Explain, how integer, real and time register data types used in verilog. (08 Marks)
- b. Show how connections between signals are specified in the module instantiation and the parts in a module definition. (08 Marks)

### Module-3

- 5 a. Discuss on And/Or Gates with respect to logic symbols, gate instantiation and truth tables. (08 Marks)
- b. Design AOI based 4:1 multiplexer, write verilog description for the same and its stimulus. (08 Marks)

OR

- 6 a. List the characteristics of continuous assignments. (04 Marks)
- b. Write the verilog description of 4 bit full adder using dataflow operators and with carry look ahead mechanism. (06 Marks)
- c. Discuss briefly available gate delays in verilog. (06 Marks)

### Module-4

- 7 a. Explain multiway branchings loops with examples. (14 Marks)
- b. Outline the characteristics of parallel blocks. (02 Marks)

OR

- 8 a. List and discuss different delay based timing control. (09 Marks)
- b. Differentiate between blocking and non blocking assignments. (07 Marks)

Module-5

- 9 a. List and explain the short comings of VHDL. (04 Marks)  
b. List the different steps of VHDL design process for design synthesis? Discuss briefly. (12 Marks)

OR

- 10 a. Write VHDL code for 4 bit comparator using behavioral description style. (05 Marks)  
b. Write VHDL code for full adder in structural description style using 2 half adders. (05 Marks)  
c. Explain scalar data types of VHDL with examples. (06 Marks)

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