CBCS SCHEME

USN | | | | | | | | | | |

15EC63

Sixth Semester B.E. Degree Examination, June/July 2019
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Derive the CMOS inverter DC characteristics graphically from p device and n device characteristics and show all operating regions. **(08 Marks)**

b. Explain the working of nMOS enhancement mode transistor with suitable diagrams. **(08 Marks)**

OR

2 a. Derive expression for drain current in linear and saturation region for nMOS transistor. **(08 Marks)**

b. With neat sketches explain the CMOs P-well process steps to fabricate a CMOS inverter. **(08 Marks)**

Module-2

3 a. Write the lambda based design rules for separation of layers and transistors. **(06 Marks)**

b. Draw circuit, stick and layout diagram for nMOS shift register cell. **(10 Marks)**

OR

4 a. Define sheet resistance (R_S) standard unit of capacitance ($\square Cg$) and delay unit (τ) **(06 Marks)**

b. Calculate the capacitance of the structure given below in Fig.Q4(b). **(10 Marks)**

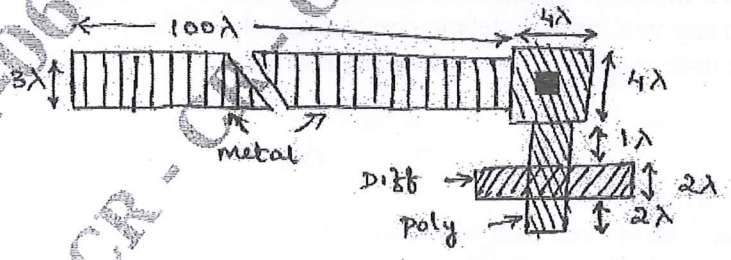

Fig.Q4(b)

Area capacitance value for metal 1 to substrate = 0.3pF × $10^{-4}/\mu m^2$(0.075 relative value)
Area capacitance value for diffusion to substrate = 1pf × $10^{-4}/\mu m^2$(0.25 relative value)
Area capacitance value for polysilicon to substrate = 0.4 pF × $10^{-4}/\mu m^2$(0.1 relative value).

Module-3

5 a. Obtain the scaling factor for the following device parameters :
   i) gate capacitance
   ii) gate area
   iii) saturation current (Idss)
   iv) channel resistance (R_{on})
   v) maximum operating frequency (f_0)
   vi) power dissipation per gate (Pg)
   vii) current density (J)
   viii) gate delay (T_d). **(08 Marks)**

b. With a neat diagram explain 4 × 4 Barrel shifter. **(08 Marks)**

OR

6 a. Explain the general arrangement of a 4 bit data path for processor. **(08 marks)**

b. Describe Manchester carry chain element. **(08 Marks)**

Module-4

7 a. Discuss the architectural issues to be followed in the design of VLSI sub system. **(05 Marks)**

b. Explain in detail the general structure of an FPGA fabric. **(06 Marks)**

c. Explain switch logic implementation of CMOS 5 way selector with neat circuit diagram. **(05 Marks)**

OR

8 a. Explain the structured design approach for the implementation of a parity generator. **(08 marks)**

b. Explain dynamic CMOS logic with example. **(08 Marks)**

Module-5

9 a. Explain 3 transistor dynamic RAM cell with schematic diagram. **(06 Marks)**

b. Explain any two fault models in combinational circuits. **(06 Marks)**

c. Write a note on automatic test pattern generation. **(04 Marks)**

OR

10 a. write short notes on :
   i) observability and controllability
   ii) Built In Self Test (BIST). **(08 Marks)**

b. Explain nMOS pseudo static RAM cell with schematic diagram. **(08 Marks)**

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