CBCS SCHEME

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15EC655

Sixth Semester B.E. Degree Examination, June/July 2019
Microelectronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive the expression of drain current of a MOS device for triode and saturation region. **(08 Marks)**

b. Consider a CMOS process for which $L_{min} = 0.4\mu m$, $t_{ox} = 8nm$, $\mu_n = 450 cm^2/v.s$ and $v_t = 0.7V$

i) Find C_{ox} and k_n^1

ii) For an NMOS transistor $\frac{W}{L} = \frac{8\mu m}{0.8\mu m}$. Calculate the values of V_{GS} and V_{DSmin} needed to operate a transistor in saturation region with a DC current $I_D = 100\mu A$.

iii) For the derive in (ii), find the value of V_{GS} required to cause the device to operate as 1000Ω resistor for a very small V_{DS}. **(08 Marks)**

OR

2 a. With the neat diagram obtain the expression for finite O/P resistance in saturation region. **(07 Marks)**

b. Define the following parameter with respect to MOSFET:
i) Threshold voltage ii) Body Effect. **(05 Marks)**

c. For the circuit shown in Fig.Q.2(c), find the values of R and V_D to obtain a current I_D of $80\mu A$. Let the NMOS transistor have $V_t = 0.6V$, $\mu_n C_{ox} = 200\mu A/V^2$, $L = 0.8\mu m$ and $W = 4\mu m$. Assume $\lambda = 0$. **(04 Marks)**

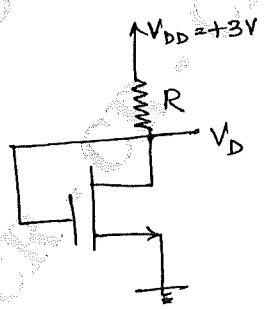

Fig.Q.2(c)

Module-2

3 a. Draw the circuit diagram of source follower amplifier. Draw its small signal equivalent circuit with r_o. Obtain the expression for R_{in}, R_{out}, A_v, A_{v_o} and Gv. **(10 Marks)**

b. List the various techniques used for biasing in MOS amplifier circuits and explain any two in detail. **(06 Marks)**

OR

4 a. Draw the development of T-Equivalent circuit model for the MOSFET. **(05 Marks)**

b. Explain the high frequency model of MOSFET with a neat diagram and internal capacitances. **(06 Marks)**

c. Derive the expression for transconductance g_m and voltage gain A_v for a common source amplifier with small input signal. **(05 Marks)**

Module-3

5 a. Determine the G_v, A_v, R_{out}, R_{in}, A_{v_o} for a common source MOS amplifier. **(08 Marks)**

b. Derive the expression for determining 3-dB frequency (W_H) of an amplifier. **(08 Marks)**

OR

6 a. Explain the operation of a MOSFET current steering circuits with necessary expressions. **(08 Marks)**

b. Fig.Q.6(b) shows an ideal voltage amplifier having a gain of -100V/V with an impedance Z is

i) A 1MΩ resistance

ii) A 1pF capacitance. In each case, use the equivalent circuit to determine V_o/V_{sig}. **(08 Marks)**

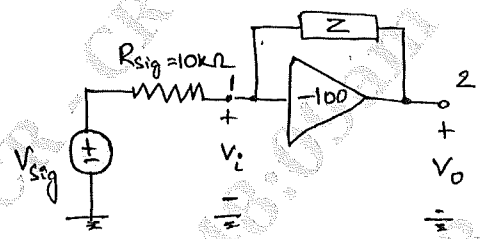

Fig.Q.6(b)

Module-4

7 a. Consider a CMOS CS amplifier in Fig.Q.7(a) for the case $V_{DD} = 3V$, $V_{tn} = |V_{tp}| = 0.6V$, $\mu_n C_{ox} = 200\mu A/V^2$, $\mu_p C_{ox} = 65\ \mu A/V^2$ for all transistors L = 0.4μm, W = 4μm. Also $V_{An} = 20V$, $|V_{AP}| = 10V$, $I_{REF} = 100\mu A$. Find g_{m1}, r_{o1}, r_{o2} and small signal voltage gain. **(06 Marks)**

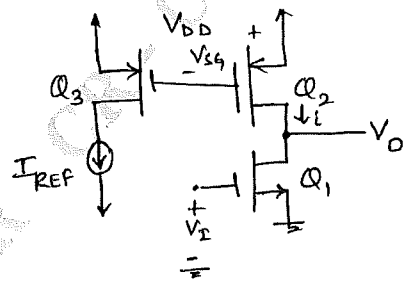

Fig.Q.7(a)

b. For a common gate amplifier with active load determine the expression for R_i, A_{vo}, A_v, G_{vo}, G_v, R_o. **(10 Marks)**

OR

8 a. Explain the following: i) Double cascode ii) Folded cascode. **(08 Marks)**

b. Explain the high frequency response of MOS cascode amplifier with necessary diagram and expressions. **(08 Marks)**

Module-5

9 a. Explain the operation of MOS differential pair with a differential input voltage. **(08 Marks)**

b. Prove that $A_{CM} = \frac{-r_{o4}}{2R_{ss}} \times \frac{1}{1+g_{m3}r_{o3}}$ for the active loaded MOS differential amplifier. **(08 Marks)**

OR

10 a. For the nMOS differential pair with a common mode voltage V_{CM} applied as shown in Fig.Q.10(a). Let $V_{DD} = V_{SS} = 2.5V$ $K_n' \frac{W}{L} = 3mA/v^2$, $V_{tn} = 0.7V$, I = 0.2mA, $R_D = 5K\Omega$.

Neglect channel length modulation

i) Find V_{OV} and V_{GS} for each transistor

ii) For $V_{CM} = 0$, Find Vs, i_{D1}, i_{D2}, V_{D1} and V_{D2}

iii) What is highest value of V_{cm} for which Q_1 and Q_2 remain in saturation, if current source I requires a minimum voltage of 0.3V to operate properly. What is the lowest value for V_s and hence for V_{cm}?

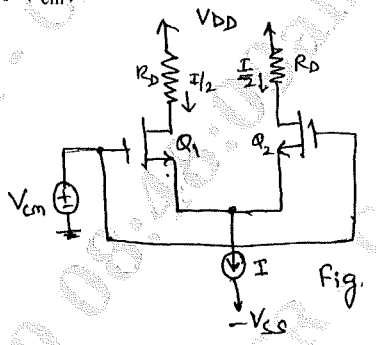

Fig.Q.10(a)

(08 Marks)

b. With neat circuit diagram, explain the operation of two stage CMOS Op-amp configuration. **(08 Marks)**

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