

Sixth Semester B.E. Degree Examination, June/July 2019
Microelectronic Circuits

Time: 3 hrs.

Max. Marks:100

Note: Answer any THREE full questions from Part-A and any TWO full questions from Part-B.

PART - A

- 1 a. With a diagram and characteristic curves, derive relationship between $i_D - V_{DS}$ and discuss the characteristics for an enhancement NMOS transistor. (10 Marks)
- b. Analyze the circuit shown in Fig.Q.1(b) to determine the voltages at all nodes and the currents through all branches. Let $V_t = 1V$, $K_n^1 \left(\frac{W}{L}\right) = 1mA / V^2$ and assume $\lambda = 0$. (05 Marks)

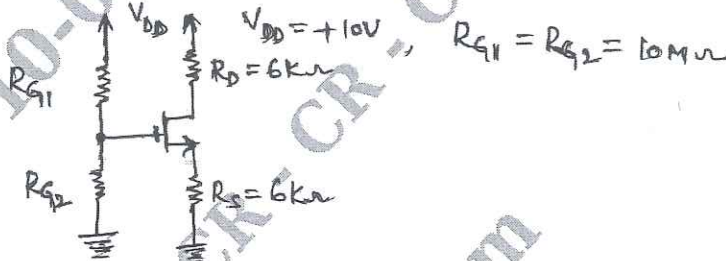


Fig.Q.1(b)

- c. Consider a process technology for which $L_{min} = 0.4\mu m$, $t_{ox} = 8nm$, $\mu_n = 450 cm^2/v.s$ and $V_t = 0.7V$,
 - i) Find C_{ox} and k_n^1
 - ii) For a MOSFET with $W/L = 8\mu m / 0.8\mu m$, calculate the values of V_{GS} and V_{DSmin} needed to operate the transistor in the saturation region with a dc current $I_D = 100\mu A$.
 - iii) For the device in (ii), find the value of V_{GS} required to cause the device to operate as a 1000Ω resistor for very small V_{DS} . (05 Marks)

- 2 a. Explain the following with the help of a diagram and waveforms:
 - i) DC bias point
 - ii) Signal current in the drain terminal
 - iii) Voltage gain. Derive appropriate equations. (10 Marks)

- b. For the devices in the circuit of Fig.Q.2(b), $|V_t| = 1v$, $\lambda = 0$, $\gamma = 0$, $\mu_n C_{ox} = 50\mu A/V^2$, $L = 1\mu m$, $w = 10\mu m$, find V_2 and I_2 . How do these values change if Q_3 and Q_4 are made to have $W = 100\mu m$? (05 Marks)

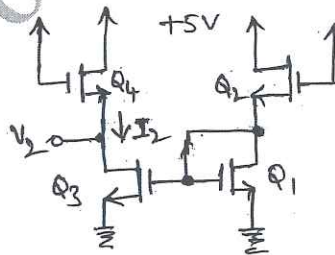


Fig.Q.2(b)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
 2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

- c. Using the feedback bias arrangement shown in Fig.Q.2(c) with a, 9V supply and NMOS device for which $V_t = 1\text{V}$, $K_n^1 \left(\frac{W}{L}\right) = 0.4\text{mA/V}^2$, find R_D to establish a drain current of 0.2mA. If resistor values are limited to those on the 5% resistor scale, what value would you choose? What values of current and V_D result? (05 Marks)

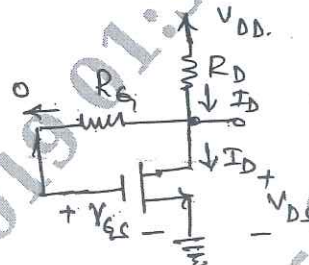


Fig.Q.2(c)

- 3 a. Discuss the IC biasing techniques with relevant diagrams and expressions. (10 Marks)
 b. Fig.Q.3(b) shows the high-frequency equivalent circuit of a common source MOSFET amplifier. For $R_{sig} = 100\text{K}\Omega$, $R_{in} = 420\text{K}\Omega$, $C_{gs} = C_{gd} = 1\text{pf}$, $g_m = 4\text{mA/V}$, $R_L' = 3.33\text{K}\Omega$, find the mid band voltage gain A_m and the upper 3-dB frequency, f_H . (06 Marks)

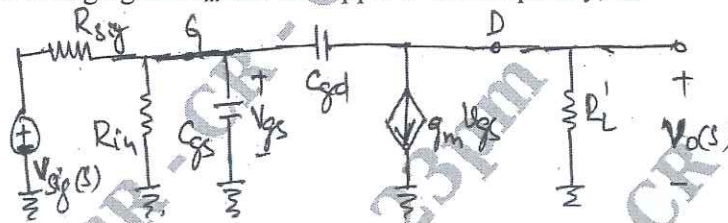


Fig.Q.3(b)

- c. With an equivalent circuit discuss Miller's theorem. (04 Marks)
- 4 a. A CMOS common-source amplifier shown in Fig.Q.4(a) has $W/L = 7.2 \mu\text{m}/0.36\mu\text{m}$ for all transistors, $\mu_n C_{ox} = 387 \mu\text{A/V}^2$, $\mu_p C_{ox} = 86 \mu\text{A/V}^2$, $I_{REF} = 100\mu\text{A}$, $V_{An}^1 = 5\text{V}/\mu\text{m}$, $|V_{AP}^1| = 6\text{V}/\mu\text{m}$. For Q_1 , $C_{gs} = 20\text{fF}$, $C_{gd} = 5\text{fF}$, $C_L = 25\text{fF}$, $R_{sig} = 10\text{K}\Omega$. Assume C_L includes all capacitances of Q_2 at the output node. Find f_H using Miller equivalence and the open circuit time constants. Also determine the exact values of f_{p1} , f_{p2} and f_z and hence provide another estimate for f_H . (09 Marks)

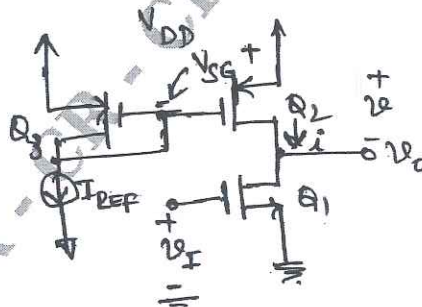


Fig.Q.4(a)

- b. Derive an expression for voltage gain and high frequency response of CG amplifier with active loads. (08 Marks)
 c. Discuss the bipolar mirror with base-current compensation. (03 Marks)

- 5 a. With diagram, derive an expression for input offset voltage of the differential pair. (07 Marks)
 b. Consider an active-loaded MOS differential amplifier shown in Fig.Q.5(b). Assume for all transistors, $\frac{W}{L} = 8.2\mu\text{m}/0.36\mu\text{m}$, $C_{gs} = 20\text{fF}$, $C_{gd} = 5\text{fF}$, $C_{db} = 5\text{fF}$. Let $\mu_n C_{ox} = 387\mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 86\mu\text{A}/\text{V}^2$, $V_{An}^1 = 5\text{V}/\mu\text{m}$, $|V_{Ap}^1| = 6\text{V}/\mu\text{m}$. Bias current $I = 0.2\text{mA}$, $R_{SS} = 25\text{K}\Omega$, $C_{SS} = 0.2\text{PF}$ and the capacitance at output node $C_x = 25\text{fF}$. Determine the low-frequency values of A_d , A_{cm} and CMRR. Also find the poles and zero of A_d and the dominant pole of CMRR. (09 Marks)

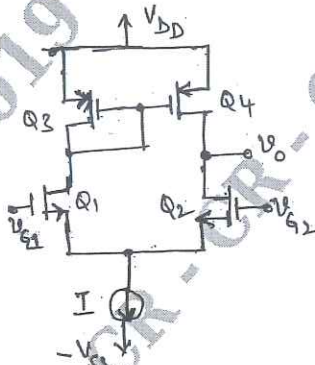


Fig.Q.5(b)

- c. With a diagram, explain the two-stage CMOS OPamp. (04 Marks)

PART - B

- 6 a. Explain the properties of negative feedback. (08 Marks)
 b. For the OpAmp circuit shown in Fig.Q.6(b), $\mu = 10^4$, $R_{id} = 100\text{K}\Omega$, $r_o = 1\text{k}\Omega$, $R_L = 2\text{K}\Omega$, $R_1 = 1\text{K}\Omega$, $R_2 = 1\text{M}\Omega$ and $R_s = 10\text{K}\Omega$. Find the values for A , β , the closed - loop gain (v_o/v_s), input resistance (R_{in}) and the output resistance (R_{out}). (07 Marks)

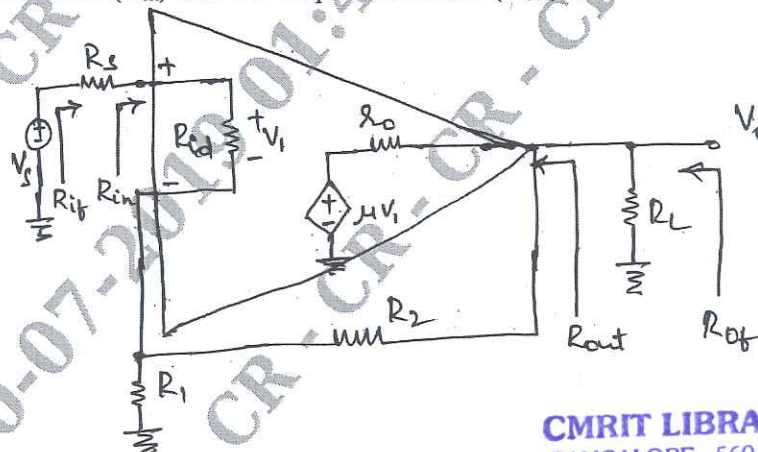


Fig.Q.6(b)

CMRIT LIBRARY
 BANGALORE - 560 037

- c. Discuss the effect of feedback on the amplifier with two-pole response. (05 Marks)
- 7 a. Discuss and derive an expression for output voltage of antilogarithmic amplifiers. (05 Marks)
 b. With a diagram, derive an expression for common mode gain of single Op-Amp difference amplifier. (07 Marks)

- c. Assuming OpAmp to be ideal, derive an expression for closed-loop gain (v_o/v_i) of the circuit shown in Fig.Q.7(c)(i). Using this circuit design an inverting amplifier with a gain of 100, input resistance of $1M\Omega$. For practical reasons, not to use the resistors greater than $1M\Omega$. Compare your design with the circuit shown in Fig.Q.7(c)(ii). (08 Marks)

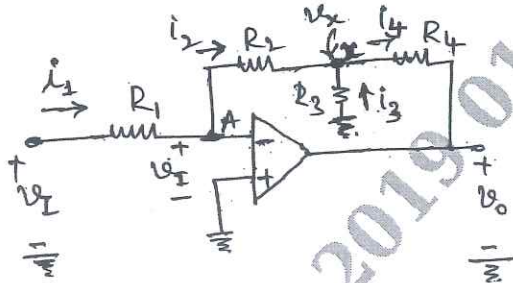


Fig.Q.7(c)(i)

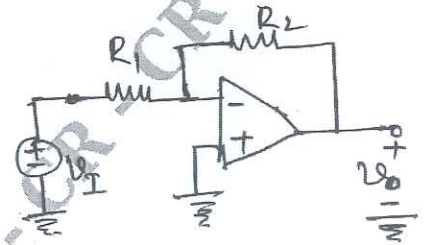


Fig.Q.7(c)(ii)

- 8 a. Explain the transistor sizing with an example of 4 input NAND gate. (06 Marks)
- b. Consider a CMOS inverter fabricated in a $0.25\mu\text{m}$ process for which $C_{ox} = 6\text{fF}/\mu\text{m}^2$, $\mu_n C_{ox} = 115\mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 30\mu\text{A}/\text{V}^2$, $V_{tn} = -V_{tp} = 0.4\text{V}$, $V_{DD} = 2.5\text{V}$. W/L ratio for $Q_N = 0.375\mu\text{m}/0.25\mu\text{m}$ and for $Q_P = 1.125\mu\text{m}/0.25\mu\text{m}$, $C_{gs} = C_{gd} = 0.3\text{fF}/\mu\text{m}$ of gate width, $C_{dbh} = 1\text{fF}$, $C_{dbp} = 1\text{fF}$ and $C_w = 0.2\text{fF}$. Find t_{PHL} , t_{PLH} and t_p . (07 Marks)
- c. Explain the parameters used to characterize the operation and performance of logic family. (07 Marks)
