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10EC666

Sixth Semester B.E. Degree Examination, June/July 2019
Digital System Design using Verilog

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. Explain design methodology with flowchart in detail. **(08 Marks)**

b. Suppose a factory has two vats, only one of which is used at a time. The liquid in the vat in use needs to be at right temperature, between 23°C and 33°C. Each vat has two temperature sensors indicating whether the temperature is above 23°C and above 33°C respectively. The vats also have low level sensors. The supervisor needs to be woken up by a buzzer when the temperature is too high too low or the vat level is too low. He has a switch to select which vat is in use. Design a circuit of gates to activate the bezzer as required. Write the verilog code for some. **(09 Marks)**

c. Suppose, for a family of logic components, $V_{IL} = 0.6V$ and $V_{IH} = 1.2V$. What voltage are required for V_{OL} and V_{OH} to provide a noise margin of 0.2V? **(03 Marks)**

2 a. Design an encoder for use in a domestic burgler alarm that has sensors for each of eight zones. Each sensor signal is '1' when an intrusion is detected in that zone, and '0' otherwise. Write a verilog code for this encoder, considering the priority such that zone 8 having the highest and zone 1 having the least. **(08 Marks)**

b. Develop a verilog model for a 7 segment decoder. Include on additional input, blank, that overrides the BCD input and causes are segments not to be lit. **(08 Marks)**

c. The alarm will ring iff (if and only if) the alarm switch is turned on and the door is not closed or if it is after 6pm and the window is not closed. Develop the verilog code for same. **(04 Marks)**

3 a. Develop a verilog model of a code converter to convert the 4 bit unsigned binary code to a 4 bit gray coded output. **(06 Marks)**

b. Explain fast carry chain adder. **(06 Marks)**

c. What numbers are represented by the following signed 2's complement fixed point numbers, assuming the binary point is four places from the right 00101100 and 11111101? **(04 Marks)**

d. Express the number 40.15625 in floating point format with 8 bits of exponent and 23 bits of Mantissa magnitude. **(04 Marks)**

4 a. Develop a verilog model for a pipelined circuit that computes the average of corresponding values in three streams of input values a, b and c. The pipeline consists of three stages: The first stage sums the value of a and b and saves the value of C; the second stage adds on the saved value of C; and the third stage divides by three. The inputs and output are all signed fixed point numbers indexed from 5 down to -8. **(06 Marks)**

b. Design a circuit that courts 16 clock cycles and produces a control signal, control that is 1 during every 9^{th} and 12^{th} cycle. Develop verilog code for same. **(10 Marks)**

c. Explain metastability. **(04 Marks)**

PART – B

5 a. Design a 64K × 8 bit composite memory using four 16K × 8 bit components. **(08 Marks)**

b. Explain : i) PROM ii) Flash memories. **(06 Marks)**

c. Using the Hamming code, determine wheather there is an error in each of the following ECC words, determine the corrected ECC word and the original data value.

i) 110111000110

ii) 100100011010 ? **(06 Marks)**

6 a. Explain the elements of embedded computer with neat diagram. **(08 Marks)**

b. Explain the signal integrity issues in PCB design, also discuss the technique for maintaining signal integrity. **(10 Marks)**

c. What do the "L" and "S" in the partname 74LS47 stands for? **(02 Marks)**

7 a. Discuss cache memory in processor. What are the advanced techniques used to enable higher rate of transfer or memory bandwidth? **(08 Marks)**

b. Suppose the value in data memory location 100 represents the number of seconds elapsed in time interval. Write instructions to increment the value, wrapping around to 0 when the value increments above 59. **(04 Marks)**

c. Explain serial interface standards in detail. **(08 Marks)**

8 a. Suppose execution time is estimated for the various parts of an algorithm on an embedded processor. The algorithm has two kernels, one that consumes 80% of execution time and another that consumes 15%. Using a hardware accelerator, we could speed up execution of the first kernel by a factor of 10 or the second kernel by a factor of 100. Which accelerator gives the best overall performance improvement? **(05 Marks)**

b. Discuss the physical design of ASIC. **(05 Marks)**

c. What is BIST technique? Explain the LFSR and CFSR with circuit diagram. **(10 Marks)**

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