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10ELN15/25

First/Second Semester B.E. Degree Examination, June/July 2018
Basic Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, choosing at least two from each part.***

PART – A

1 a. Choose the correct answers for the following : **(04 Marks)**

i) Insulator has _____ temperature coefficient of resistance
A) Negative B) Positive C) high D) Low

ii) The energy required in capturing the electron is _____ for silicon
A) 5eV B) 0.5eV C) 50eV D) 0.05eV

iii) The TUF of a HWR is _____
A) 0.278 B) 2.87 C) 0.287 D) 287

iv) The PIV of a FWR is _____
A) $2V_m$ B) V_m C) $V_m - V_t$ D) 2V

b. A Full wave bridge rectifier is driving a resistive load of 50Ω and supply of 230V, 50Hz. Assume diode resistance is zero. Determine:
(i) DC output voltage (ii) Average value of current (iii) ripple factor. **(08 Marks)**

c. What is Filter? And why capacitor filter is commonly used? **(04 Marks)**

d. Draw the AC equivalent circuit of a diode. **(04 Marks)**

2 a. Choose the correct answers for the following : **(04 Marks)**

i) _____ is a control terminal in a transistor, which controls the large current flowing from emitter to collector.
A) Emitter B) Base C) Collector D)Emitter base

ii) The collector current in a transistor is 5mA, and Base current of 35μA. If β = 140, calculate the value of leakage current F_{CBO}
A) 0.709 mA B) 7.09 mA C) 10 mA D) 7 mA

iii) The phase relation between input and output of a CE – configuration is _____
A) Inphase B) 90° C) 160° D) out of phase.

iv) The transistor is required to be operated as a switch, then it should be operated in
A) Cutoff B) Saturation
C) Saturation and cutoff D) Middle.

b. Draw the input and output characteristics of a CB – configuration of a transistor and explain it. **(08 Marks)**

c. Determine Q-point values for the circuit shown in Fig. Q2 (c). Assume β = 100 and V_{BE} = OV **(04 Marks)**

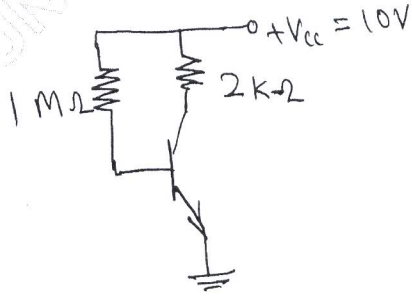


Fig Q2(c)

d. Compare CE with CB – configuration of a Transistor. **(04 Marks)**

3 a. Choose the correct answers for the following : **(04 Marks)**

i) Larger the value of stability factor, the circuit will exhibit _____
A) Stable B) Instability C) highly stable D) Linear.

ii) I_{CBO} is doubles for every _____ changes in temperature
A) 100°C B) 1000°C C) 11°C D) 10°C.

iii) _____bias circuit is commonly used
A) Voltage divider B) Fixed bias C) Collector bias D) Emitter bias.

iv) _____ is a process of making the Q-point independent of temperature changes or variation in transistor parameters.
A) Thermal B) Q-point C) Stabilization D) Biasing.

b. For the voltage divider biasing circuit with $R_1 = 47k\Omega$, $R_2 = 15\ k\Omega$, $R_c = 1.5\ k\Omega$, $R_E = 1\ k\Omega$, $V_{CC} = 15V$ and $V_{BE} = 0.7V$. Calculate emitter voltage, collector voltage and V_{CE}. **(08 Marks)**

c. What are factors causes instability of a Q-point and explain it. **(08 Marks)**

4 a. Choose the correct answers for the following : **(04 Marks)**

i) Latching current of an SCR is ____ holding current
A) Lower than B) Equal to C) Smaller D) higher than

ii) UJT is called as _____ oscillator.
A) Auxiliary B) Relaxation C) Sinewave D) Square wave

iii) Input impedance of a JFET is _____
A) high B) Low C) Medium D) 10 kΩ

iv) The unit of trans conductance is _____
A) Volts B) Amp C) Volts/Amp D) mA/volts.

b. Draw the VI – characteristics of an SCR and explain it. Mention application of SCR. **(08 Marks)**

c. Draw the circuit diagram and waveforms of a UJT relaxation oscillation and explain it. **(08 Marks)**

PART – B

5 a. Choose the correct answers for the following : **(04 Marks)**

i) The voltage gain of a amplifier is 100000 can be represented in _____ dBs.
A) 10 B) 100 C) 1000 D) 101.

ii) A single stage amplifier having gain of 60dB, if the input signal is 10mV, what will be the output voltage?
A) 1V B) 1000V C) 100V D)10V

iii) The feedback network in a amplifier circuit produces ____ phase.
A) 180° B) 0° C) 360° D) 90°.

iv) For over damped type oscillation Aβ must be _____ one
A) Less than B) Equal to C) Greater than D) Less.

b. Draw the circuit diagram of a transistorized RC – phase shift oscillator and explain it. **(08 Marks)**

c. A crystal has L = 2H, C = 0.01pF and R = 2kΩ, its mounting capacitance is 2pF. Calculate its series and parallel resonant frequency. **(05 Marks)**

d. What is the need for cascading of Amplifier? **(03 Marks)**

6 a. Choose the correct answers for the following : **(04 Marks)**

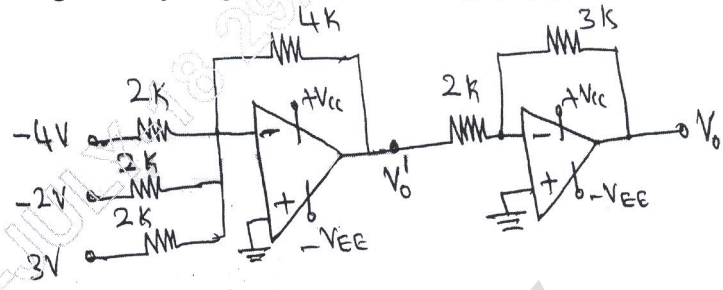
i) The unit of slew rate of an op-amp is _____
A) V/sec B) V/μsec C) A/μsec D) Sec

ii) The Bandwidth of an practical op-amp under open loop configuration is _____
A) Larger B) Infinity C) 2000 D) very small

iii) The number of electrons present in electron beam of a CRT is controlled by _____
A) Control grid B) Base C) Anode D) Deflection system

iv) _____ is used to generate saw tooth waveform required to deflect the beam in horizontal section of CRO.
A) Generator B) Time base generator C) Crystal D) Amplifier.

b. Find the output voltage of a op-amp circuit show in Fig Q6(b). **(06 Marks)**



FigQ6(b)

c. Draw the block diagram of a CRO and mention functions of each block. **(07 Marks)**

d. List the ideal characteristics of an op-amp. **(03 Marks)**

7 a. Choose the correct answers for the following : **(04 Marks)**

i) The modulation index value of a AM for proper modulation should be _____
A) less than one B) zero C) more than one D) 100.

ii) $(11101110101)_2 = (\ ?\ )_8$
A) 3566 B) 3560 C) 3565 D) 3567.

iii) $(9CF1)_{16} = (\ ?\ )_{10}$
A) 40170 B) 40176 C) 40177 D) 40175.

iv) The output frequency of a mixer of super heterodyne receiver is _____
A) 454 KHz B) 455 KHz C) 455 MHz D) 100 KHz.

b. Compare AM with FM signals. **(04 Marks)**

c. Perform the following: i) $(57.6)_8 = (\ ?\ )_2 = (\ ?\ )_{16}$ ii) $(193)_{16} = (\ ?\ )_8 = (\ ?\ )_{10}$. **(08 Marks)**

d. Consider a 600W, 120 KHz carrier modulated to depth of 60% by modulating signal of 1KHz. Calculate total power transmitted and frequency of side band. **(04 Marks)**

8 a. Choose the correct answers for the following : **(04 Marks)**

i) A(B +C) = AB + AC is a _____ property
A) Distributive B) Associative C) Duality D) Commutative.

ii) _____ Gate output is at logic zero, when all the inputs are at logic one
A) AND B) OR C) NAND D) NOR.

iii) _____ gate is a combination of EX-OR gate followed by NOT-Gate
A) NAND B) EX-NOR C) NOR D) EX-OR

iv) Simplification of AB + ABC + ABD + ABE is _____
A) A B) BC C) BCD D)AB.

b. Simplify the following boolean expressions

i) $Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C} + A\,B\,\overline{C}$

ii) $Y = \overline{A}(B + \overline{C})(A + \overline{B} + C)(\overline{\overline{A}\,\overline{B}\,\overline{C}})$ **(08 Marks)**

c. Design a full adder circuit and realize using two half adder. **(08 Marks)**

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