CBCS SCHEME

USN | | | | | | | | | | |

15ELN15/25

First/Second Semester B.E. Degree Examination, June/July 2019
Basic Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Draw forward and reverse V- I, characteristics of Si and G_e diodes and make any two comparison between Si and G_e diodes. **(04 Marks)**

b. With a neat circuit diagram, input and output waveforms, explain the working of an Half wave diode rectifier. **(06 Marks)**

c. A full-wave rectifier supplies a load of 1000Ω. The ac voltage applied to it is 200-0-200 V(rms). Calculate i) I_{Dc} ii) I_{rms} iii) efficiency (η), Assume $R_f = 0\Omega$. **(06 Marks)**

OR

2 a. Define 'α' and 'β' of a transistor amplifier and derive the relation between α and β. **(04 Marks)**

b. With a neat circuit diagram, input and output waveforms, explain the operation of a Full wave two diode rectifier. **(06 Marks)**

c. Draw an output characteristics of CE-transistor amplifier, mark different regions of working on it, explain each region of working. **(06 Marks)**

Module-2

3 a. With a neat sketch and equations, explain what is dc load line and bias point in a CE base bias amplifier. **(04 Marks)**

b. Explain with neat circuit diagram and equations, voltage divider bias amplifier. **(06 Marks)**

c. Design bas-bias transistor circuit, using 'Si' transistor having 'β' value of 100, V_{CC} is 10V, and dc bias conditions are to be $V_{ce} = 5v$ and $I_c = 5mA$. **(06 Marks)**

OR

4 a. Define CMRR and slew rate and write any four ideal characteristics for op-amp. **(04 Marks)**

b. With a neat circuit diagram, derive an equation for op-amp application as
i) Inverting amplifier ii) Non-inverting amplifier
iii) Inverting 2-input summer iv) Subtractor
v) Integrator vi) Differentiator. **(12 Marks)**

Module-3

5 a. Convert $(1101010)_2 = (\ )_{10}$ and $(65)_{10} = (\ )_2$ **(04 Marks)**

b. Convert $(ABCD)_{16} = (\ )_8$ and $(16000)_8 = (\ )_{16}$ **(04 Marks)**

c. Write the truth table, design equations and circuit diagram of an Half adder using logic gates. **(08 Marks)**

OR

6 a. State and prove De Morgan's Theorem for 3-variables. **(04 Marks)**

b. Realize AND, OR and EX-OR gates using NAND gates. **(06 Marks)**

c. Perform the following subtraction using 1's and 2's complement, $(10111001)_2 - (1011)_2$. **(06 Marks)**

Module-4

7 a. Compare flip-flop and Latch. **(02 Marks)**

b. With circuit diagram and truth table explain the working of a NAND gate latch. **(07 Marks)**

c. Explain the operation of clocked RS-flip flop, with circuit diagram and truth table. **(07 Marks)**

OR

8 a. Explain with circuit diagram and truth table working of NOR gate latch. **(06 Marks)**

b. Draw the architecture of 8051 microcontroller, explain the function of each block used in it. **(10 Marks)**

Module-5

9 a. Draw the block diagram of communication system, explain the functions of each block used in it. **(05 Marks)**

b. Define amplitude modulation and derive equation of amplitude modulated double side band wave. **(05 Marks)**

c. A carrier of 2MHz has 1kW of its power amplitude modulated with a sinusoidal signal of 2KHz, the depth of modulation is 60%. Calculate the side band frequencies, signal band width, power in side bands, and total power of modulated wave. **(06 Marks)**

OR

10 a. Distinguish between active and passive transducers. **(02 Marks)**

b. Bring out any four differences between amplitude modulation and frequency modulation. **(04 Marks)**

c. Explain with neat diagram working of LVDT. **(10 Marks)**

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