CBCS Scheme

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15EE35

# Third Semester B.E. Degree Examination, Dec.2016/Jan.2017
## Digital System Design

Time: 3 hrs. Max. Marks: 80

**Note: Answer any FIVE full questions, choosing one full question from each module.**

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

### Module-1

1 a. Simplify the following Boolean function using K-map.
$f(v, w, x, y, z) = \Sigma m (3, 7, 8, 10, 11, 12, 14, 15, 17, 19, 21, 23, 25, 27, 29, 31) + \Sigma d (2, 6, 26, 30)$. **(08 Marks)**

b. Simplify the boolean expression using a 3-variable VEM with'd' as MEV.
$f(a, b, c, d) = \Sigma m (1, 3, 7, 11, 15) + \Sigma d (0, 2, 5)$. **(08 Marks)**

**OR**

2 a. Using Quine –McCluskey method, obtain a minimal sop expression of,
$f(w, x, y, z) = \pi m (0, 4, 5, 9) \cdot d (1, 7, 13)$. **(10 Marks)**

b. Find minimal sop expression using VEM with 'c' as MEV.
$f(a, b, c, d) = \Sigma m (3, 4, 5, 7, 8, 11, 12, 13, 15)$. **(06 Marks)**

### Module-2

3 a. Realize the following Boolean function using a 8:1 MUX with wyz as select inputs.
$f(w, x, y, z) = \Sigma m (0, 1, 2, 5, 7, 8, 9, 12, 13)$. **(06 Marks)**

b. Design a 1-bit comparator using 2-4 decoder giving three outputs, G, E and L. **(04 Marks)**

c. Design a carry look ahead 4-bit parallel adder. Show that the time for addition is independent of the length of operands. **(06 Marks)**

**OR**

4 a. Implement a full subtractor using a 4:1 multiplexer. **(06 Marks)**

b. Design a 4 to 16 decoder by cascading 2 to 4 decoders. **(05 Marks)**

c. Explain a 4 to 2 line priority encoder with active high inputs and outputs using function table. **(05 Marks)**

### Module-3

5 a. Analyse the application of SRFF as switch debouncer with waveforms. **(03 Marks)**

b. Applying 4-bit shift register, design a 4-bit twisted ring counter. **(05 Marks)**

c. Design a synchronous counter with counting sequence 3, 2, 5, 1, 0, 3 . . . . Using T.FF. **(08 Marks)**

**OR**

6 a. Explain race around condition. How is it eliminated? **(04 Marks)**

b. Design and implement a divide by -10 asynchronous counter using T-FFs. **(05 Marks)**

c. Design a synchronous counter to give a counting sequence 0, 2, 3, 1, 0 . . . using J.K FF. **(07 Marks)**

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## Module-4

7 a. Construct a sequential logic circuit with single input and single output by obtaining the state and excitation table for the given state diagram using JK FF. **(08 Marks)**

b. Analyze the following sequential circuit and obtain excitation, transition and state table. Also write the state diagram. **(08 Marks)**

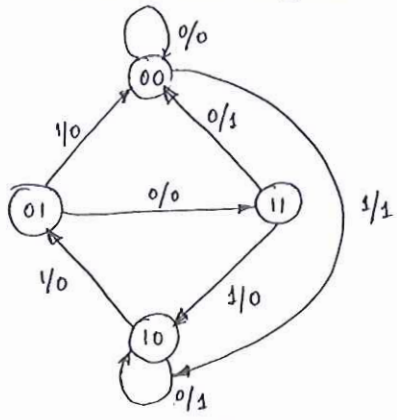


Fig Q7(a)

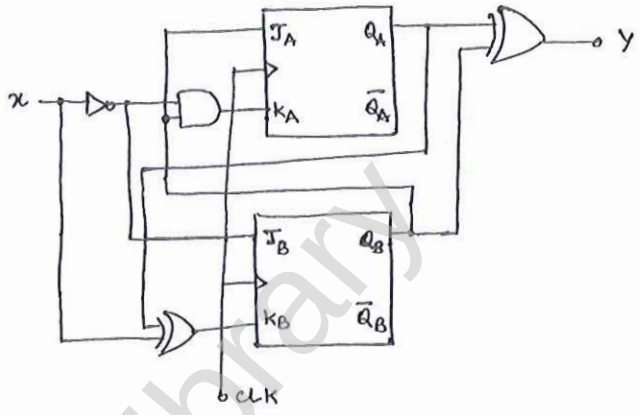


Fig Q7(b)

**OR**

8 a. By analyzing the sequential circuit obtain the equations for input a hence determine the excitation table, state table and state diagram. **(06 Marks)**

b. Design the sequential logic circuit for a single input and single output system from the state diagram using JKFF. Analyze through state table and excitation table. **(10 Marks)**

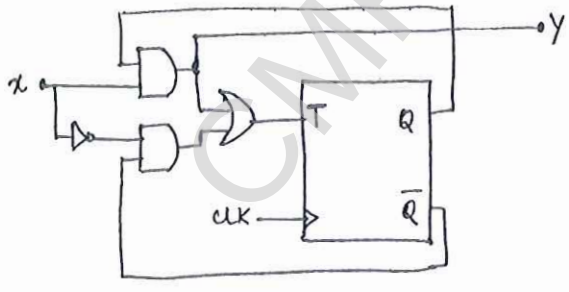


Fig Q8(a)

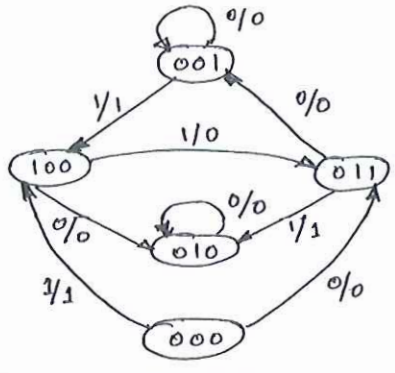


Fig Q8(b)

## Module-5

9 a. Explain entity and architecture with reference to VHDL code of full adder circuit. **(06 Marks)**

b. Write VHDL code using a process and case statement to implement 4:1 multiplexer. **(04 Marks)**

c. Implement a T-FF with active low asynchronous inputs and clock input in VHDL. **(06 Marks)**

**OR**

10 a. Explain various data types available in VHDL. **(06 Marks)**

b. Implement a single – bit comparator for all input combinations in VHDL. **(04 Marks)**

c. Write VHDL code for edge triggered JKFF with active low asynchronous inputs. **(06 Marks)**

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