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10EC45

Fourth Semester B.E. Degree Examination, Dec.2016/Jan.2017
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain composite VHDL and verilog data types. **(08 Marks)**

b. If A, B and C are the unsigned variables with A = "110011", B = "010100", C = "101". Find the values of

(i) Y = &A (ii) Y = A && B (iii) Y = A sra 2

(iv) Y = B rol 2 (v) Y = A << 2 (vi) Y = A and not B xor 2 nand C **(07 Marks)**

c. Write the major differences between VHDL and verilog. **(05 Marks)**

2 a. Write a VHDL program in data flow style using signal assignment statements to implement a 2 to 1 multiplexer with active low enable signal (Ebar). If the propagation delay of each gate is 9 ns, calculate at what time the output is available when the input signals (A, B, select, Ebar) are changed at T_0, T_1 and T_2 as shown in Fig.Q2(a). **(07 Marks)**

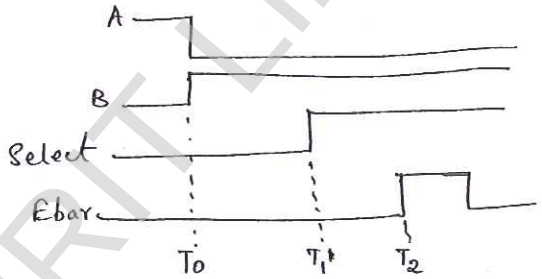

Fig.Q2(a)

b. Write a VHDL program to realize a D-latch in Data flow style, Consider enable signal as active low. **(06 Marks)**

c. Write a verilog program to implement a 3-bit carry-look ahead adder in data flow style. **(07 Marks)**

3 a. Compare signal and variable assignment statement. **(05 Marks)**

b. Write a verilog code to implement a positive edge triggered JK flip flop shown in Fig.Q3(b) in behavioural style using (i) else if and (ii) case statement. **(08 Marks)**

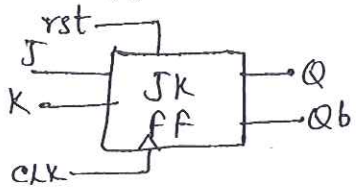

Fig.Q3(b)

c. Write the flow chart of Booth multiplication algorithm. Show the steps to find the product of two signed 5-bit numbers –5 and 9. **(07 Marks)**

4 a. Write a VHDL program to realize the block diagram shown in Fig.Q4(a) in structural style (No need to show the implementation of components). **(07 Marks)**

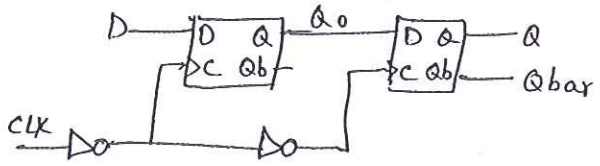

Fig.Q4(a)

b. Write a verilog program to implement a 4-bit magnitude comparator using 4-bit adders in structural style. **(07 Marks)**

c. Explain the following keywords (i) Generate (ii) Generic and (iii) Parameter. **(06 Marks)**

PART – B

5 a. Explain procedure with syntax and example in VHDL. **(06 Marks)**

b. Write a verilog program to convert an unsigned binary to an integer using task. **(08 Marks)**

c. Write a VHDL function to find the greater of two signed numbers. **(06 Marks)**

6 a. When mixed type description is preferred? Give example. **(06 Marks)**

b. Explain different VHDL user defined types. **(06 Marks)**

c. Write a verilog description of a 32×8 SRAM to implement the function table shown in Table 6(c).

CS	R/$\overline{WR}$	Memory Function
0	X	Deselected
1	1	Read cycle
1	0	Write cycle

Table 6(c) **(08 Marks)**

7 a. Explain how to invoke a VHDL entity from a verilog module. **(08 Marks)**

b. Write the block diagram of a 9-bit adder and implement it by mixed language description. **(12 Marks)**

8 a. What is synthesis? With a neat flow chart explain the steps involved in a synthesis process. **(10 Marks)**

b. Find the gate-level mapping for the verilog code given below:

```
module if_st(a, y)
input[2:0] a;
output y;
reg y;
always (a)
  begin
    if (a < 3' b 1 0 1)
      y =1' b 1;
    else
      y = 1' b 0;
    end
end module
```

(10 Marks)

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