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10EC666

Sixth Semester B.E. Degree Examination, Dec.2016/Jan.2017
Digital System Design using Verilog

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With the help of neat flow chart, describe the design methodology for hardware/software co design. **(08 Marks)**

b. Devise a circuit for a simple bungler alarm that activates a siren if either a motion detector detects motion or a sensor on a window defects that the window is open. **(05 Marks)**

c. Develop a sequential circuit that has a single data input signal 'S' and produces an output Y. The output is 'I' whenever 'S' has the same value over 3 successive clock cycles and 'O' otherwise. Assume that the value of 'S' forgiven clock cycle is defined at the time of the rising clock edge at the end of the clock cycle. **(07 Marks)**

2 a. Devise a minimal length binary code to represent the stat of the phone : on – hook, dial tone, dialing busy, connected, disconnected, ringing. Busy connected, disconnected, ringing. Write a Boolean equation involving the bits of the code that determine the phone is off hook (state other than on hook or ringing).
Develop a verilog model for a circuit that has an input representing the state of phone and an output that is 'I' when the phone is off hook. **(08 Marks)**

b. Develop a verilog code for a 7 segment decoder include an additional input "Blank" that over sides the BCD input and causes all segments not to be it. **(06 Marks)**

c. Explain state encoding with an example. **(06 Marks)**

3 a. Write a verilog code for 4 bit carry look ahead adder. **(08 Marks)**

b. Develop the verilog code for the following Fig Q3(b) the input and output codes are for number 0 – 9. **(06 Marks)**

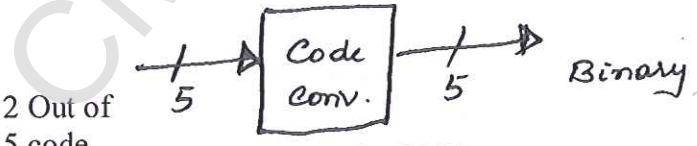

Fig Q3(b)

c. Explain how fixed point numbers are represented in verilog. **(06 Marks)**

4 a. Design a circuit that counts 16 clock cycles and produces a control signal 'ctrl' that is '1' during every eighth and twelfth cycle. Develop a verilog model of the circuit. **(08 Marks)**

b. Define the terms : setup time, hold time, clock to output time of flip flop. Illustrate with waveforms. **(04 Marks)**

c. Develop a verilog model of a pipelined circuit that computer the maximum of corresponding values in three streams of input values a, b and c. the pipeline should have two stages. First stage determines the larger of a and b and saves the value of C : the second stage finds the larger of C and the maximum of a and b. the input and outputs are all 14 bit signed 2' is complement integers. **(08 Marks)**

PART – B

5 a. Develop a verilog model of a dual port, 4k×16 bit flow through SSRAM. One port allows data to be written and read while the other port only allows data to be read. **(06 Marks)**

b. Compute the 12 bit ECC word corresponding to the 8 bit data word '0110001'. Determine whether there is an error in the ECC word '110111000110' and if so, correct it. **(08 Marks)**

c. Write a note on ASIC. **(06 Marks)**

6 a. Draw the block diagram of elements of an embedded computer and expalin the various blocks. **(10 Marks)**

b. Write the verlog module definition of memory interface signals of the Gumnelt core. Explain the signals briefly. **(05 Marks)**

c. Write a Gumnelt assembly language program to find greater to two values. **(05 Marks)**

7 a. Explain the following serial interface standards for connecting I/O devices.

i) RS – 232
ii) I^2C
iii) USB **(12 Marks)**

b. Show how a 64 bit data word can be transmitted serially between two ports of a system. Assume that the transmitter and the receiver are both within the same clock domain and that the signal start is set to 'I' on a clock cycle in which data is ready to be transmitted. **(08 Marks)**

8 a. Explain the term "Design Optimization" highlighting on the area, timing and power optimizations. **(10 Marks)**

b. Write a short notes on the

i) Boundary seam
ii) 4 bit LFSR
iii) Fault model and Fault simulation
iv) Functional verification. **(10 Marks)**

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