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10TE74

Seventh Semester B.E. Degree Examination, Dec.2016/Jan.2017
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. What is digital signal processing? What are the important issues to be considered in designing and implementing a DSP system? Explain in detail. **(09 Marks)**

b. Define decimation and interpolation process, explain them using block diagrams and equations. **(06 Marks)**

c. The signal sequence x(n) = [0, 2, 4, 6, 8] is interpolated using the interpolation filter sequence b_k = [0.5, 1, 0.5] and the interpolation factor is 2. Determine the interpolated sequence y(m). **(05 Marks)**

2 a. Explain : i) Circular addressing mode ii) Parallelism iii) Guard bits. **(06 Marks)**

b. Explain the operation of barrel shifter with example. **(07 Marks)**

c. With neat diagram, explain ALU of the DSP system. **(07 Marks)**

3 a. Explain functional architecture of TMS 320 C54XX processor with block diagram. **(10 Marks)**

b. Explain the addressing modes of TMS320C54XX processor with examples. **(10 Marks)**

4 a. Explain the pipelining operation of TMS 320 C54XX processor. **(08 Marks)**

b. Explain the operation of serial I/O ports and hardware timer of TMS320C54XX on chip peripherals. **(08 Marks)**

c. Describe the operations of the following instructions with respect to C54XX processor :
i) MAS * AR3 –, * AR4 +, B, A
ii) MPY # 01234, A. **(04 Marks)**

PART – B

5 a. With the help of block diagram, explain the implementation of an IIR filter in TMS320C54XX processor. Show the memory organization of the filter implementation. **(08 Marks)**

b. Write a TMS320C54XX program that illustrate the implementation of interpolating FIR filter of length 15 and interpolating factor 5. **(08 Marks)**

c. What is the drawback of using linear interpolation for implementing interpolation filter? Explain the scheme that overcomes this drawback. **(04 Marks)**

6 a. Write a TMS320C54XX program that illustrate the implementation of 8-bit point DIT-FFT algorithm. **(12 Marks)**

b. Briefly explain scaling and derive expression for optimum scaling factor for DIT–FFT butterfly algorithm. **(08 Marks)**

7 a. Design a data memory system with address range 7FF800h –7FFFFFh for a C5416 processor use 2K×8 SARM memory chip. **(10 Marks)**

b. Discuss in detail the interrupt handling in the C54XX processor. **(10 Marks)**

8 a. Explain briefly building blocks of PCM 3002 codec device. **(08 Marks)**

b. What do you understand by a DSP based biotelemetry receiver? **(04 Marks)**

c. With a help of a block diagram, explain JPEG algorithm. **(08 Marks)**

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