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10EC666

Sixth Semester B.E. Degree Examination, June/July 2016
Digital System Design using Verilog

Time: 3 hrs. Max. Marks:100

Note: *Answer FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1 a. What are the effects of capacitive loading and propagation delay on signal transitions between logic levels? **(10 Marks)**

b. Develop a sequential circuit that has a single data input signal 'S' and produces an output 'Y'. The output is '1' whenever 'S' has the same value over three successive clock cycles, and '0' otherwise. Assume that the value of 'S' for a given clock cycle is defined at the time of the rising clock edge, at the end of the clock cycle. **(10 Marks)**

2 a. Devise a minimal – length binary code to represent the state of a phone: on-hook, dial tone, dialing, buses, connected, disconnected, ringing. Write a Boolean equation involving the bits of the code that determines when the phone is off-hook (state other than on hook or ringing). Develop a verilog model for a circuit that has an input representing state of the phone and an output that is 1 when the phone is off-hook. **(10 Marks)**

b. Implement the Boolean function $F = (a + b\bar{c})\ (\bar{b}c)$, draw its circuit implementations. Show how Boolean function F can be transformed into SOP form. Use laws for Boolean algebra for reduction and implementation in SOP. **(10 Marks)**

3 a. With necessary equations explain fast-carry-chain full adder cells used in an adder. **(10 Marks)**

b. Explain the operation of resizing signed integers. **(06 Marks)**

c. What number is represented by the fixed point binary number 01100010, assuming the binary point is 6 places from right? **(04 Marks)**

4 a. Describe the operation of latch with timing diagram and verilog model. **(06 Marks)**

b. Design a control sequence for the control signals of the sequential complex multiplier and develop verilog model. **(10 Marks)**

c. Describe Finite State Machines (FSM) with schematic representation. **(04 Marks)**

PART – B

5 a. Develop a verilog model of a dual-port 4k × 16 – bit flow-through SSRAM. One port allows data to be written and read while the other port only allows data to be read. **(10 Marks)**

b. Determine whether there is an error in the ECC word 000111000100, and if so, correct it. **(05 Marks)**

c. If memory has 32, 768 locations, each of 32 bits what is the total capacity of the memory, and how many address bits does it require? **(05 Marks)**

6 a. What is field programmable gate arrays (FPGA)? With a diagram explain the internal organization of an FPGA. **(10 Marks)**

b. Explain differential signaling. **(10 Marks)**

7 a. With a neat diagram, explain the elements of an embedded computer, also bring out the difference between micro processor and microcontroller. **(10 Marks)**

b. What are the different techniques enabling higher rate of data transfer or memory bandwidth. **(10 Marks)**

8 a. Briefly explain the serial interface standards for I/O device. **(10 Marks)**

b. Explain the mechanism for input/output controllers to request an interrupt. **(10 Marks)**

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