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10TE74

Seventh Semester B.E. Degree Examination, June/July 2016
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: *Answer FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1 a. What is meant by a multirate system? Explain the role of decimation and interpolation in such systems. **(08 Marks)**

b. The sequence x(n) = {0, 3, 6, 9, 12} is interpolated using interpolation sequence $b_k = \left\{\frac{1}{3}, \frac{2}{3}, 1, \frac{2}{3}, \frac{1}{3}\right\}$ and the interpolation factor of 3, find the interpolated sequence y(m). **(06 Marks)**

c. Describe the basic features that should be provided in the DSP architecture to be used to implement the N^{th} order FIR filter

$$y(n) = \sum_{i=0}^{N-1} h(i)x(n-i); \quad n = 0, 1, 2, \ldots..$$

where x(n) denotes the input samples, y(n) the output sample and h(i) denotes i^{th} filter coefficients. **(06 Marks)**

2 a. Give the structure of a 4 × 4 Braun multiplier, explain its concept. What modification is required to carry out multiplication of signed numbers? **(10 Marks)**

b. What is meant by circular addressing mode? Write pointer updating algorithm for the circular addressing mode and show different cases that encounter during the updating process of the pointer. **(10 Marks)**

3 a. Describe the multiplier/adder unit of TMS320C54XX processor with neat block diagram. **(06 Marks)**

b. Explain dual operand addressing and accumulator addressing as applied to C54XX processor with an example. **(08 Marks)**

c. Explain in brief status register 0, status register 1 of C54XX. **(06 Marks)**

4 a. Describe any five assembly directives of C54XX. **(06 Marks)**

b. Describe the operation of hardware timer with a neat diagram. **(06 Marks)**

c. Explain with figure the pipeline operation of the following sequence of instruction, if the initial values of AR1, AR3, A are 204, 201, 2 and the values stored in the memory locations 201, 202, 203, 204 are 4, 6, 8, 12. Also provide the values of registers AR3, AR1, T and accumulator after completion of each cycle.

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ADD  *AR3+, A
LD   *AR1+, T
MPY  *AR3+, B
ADD  B, A
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(08 Marks)

PART – B

5 a. Describe the importance of Q-notation in DSP algorithm implementation with examples. What are the values represented by 16-bit fixed point number $N_1 = 4D00$ and $N_2 = BDAF$ in Q7 and Q15 notations. **(10 Marks)**

b. Write an assembly language program for TMS320C54XX processor to implement an FIR filter. **(10 Marks)**

6 a. Explain a general DIT-FFT butterfly in-place computation with necessary equations which is implemented in C54XX DSP. **(06 Marks)**

b. What is the need for scaling of inputs? Derive the scaling required in FFT calculation. **(06 Marks)**

c. Explain how the bit reversed index generation can be done in 8 point DIT-FFT. Write an assembly language program for 8-point DIT-FFT bit reversed index generation. **(08 Marks)**

7 a. Design a circuit to interface 64K words of program memory space from 0FFFFFh for the 5416 processor using 16K × 16 memory chips. **(10 Marks)**

b. What is an interrupt? With a neat flow chart, explain the response of C54XX to an interrupt. **(10 Marks)**

8 a. Explain how PPM signal is decoded at the receiver end using DSP. **(06 Marks)**

b. Explain the synchronous serial interface between the C54XX and a CODEC device. **(06 Marks)**

c. With a neat diagram, explain JPEG coding and decoding. **(08 Marks)**

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