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10CS74

Seventh Semester B.E. Degree Examination, Dec.2016/Jan.2017
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define the term-instruction set architecture. In what way computer architecture is related to ISA? Correlate them. **(04 Marks)**

b. Elaborate the different parameters that decide the cost of an IC. Give the equation of each parameter separately and explain them. **(06 Marks)**

c. Define the term-CPI and derive the equation for finding the total number of processor cycles needed to execute a program. Consider the execution of an object code with 200,000 instructions on a 20MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction is given below based on the result of a program trace experiment.

Sl. No.	Instruction type	C.P.I.	Instruction mix
1	Arithmetic and logic	1	68%
2	Load/store with cache hit	2	8%
3	Branch	4	14%
4	Memory reference with cache hit	8	10%

i) Find the total number of cycles required to execute the program.

ii) Calculate the average C.P.I. when the program is executed on a uniprocessor system with the above trace results.

iii) Calculate the corresponding MIPS rate based on the CPI obtained in (i) above. **(10 Marks)**

2 a. Discuss the various kinds of data dependencies that can cause problems to the smooth flow of instructions through pipelines. Give supporting example in each case and explain with an example how these dependencies can be eliminated. **(10 Marks)**

b. Explain the principles of loop unrolling. Demonstrate the normal loop execution and loop unrolling concepts for the following C-code segment by translating the given code segment given below, to MIPS assembly language code.

C – code: for (i = 1000; i > 0; i = i – 1) X[i] = X[i] + s where s = scalar value.

i) Calculate the number of clock cycles required per element for both unscheduled and scheduled loops in normal case considering stalls/idle clock cycles.

ii) Repeat the above step for loop unrolled execution case with and without schedule.

iii) Calculate the average value of clock cycles per element for the (i) and (ii). **(10 Marks)**

3 a. With reference to Branch Target Buffers (BTBs) explain.

i) The purpose of each B.T.B. entry and

ii) The meaning of the following terms and the subsequent action taken for each of the following occurrence of events.

Case(1): Branch entry found in BTB entry and predicted branch not taken. Case(2): Branch entry found in BTB entry and predicted branch not taken. **(08 Marks)**

b. Name the different techniques used for getting high performance of pipelines with multiple delivery techniques. What are integrated instruction Fetch units (IIFU)? Highlight on the basic function of such fetch units. **(08 Marks)**

c. Compare register Re-naming technique with that of Re-order buffer technique in speculation concept. **(04 Marks)**

4 a. With appropriate timing diagrams, explain the concept of delayed branch technique used in RISC processors. What are its limitations and demonstrate the scheduling of branch delay with suitable examples. **(10 Marks)**

b. Explain what is branch penalty? Discuss the different techniques used to reduce branch penalties. **(06 Marks)**

c. Consider a non-pipelined processor in RISC. Assume that it has 1ns clock cycle and that it uses 4 cycles for ALU operations and branches and 5 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose that due to clock skew and set up, pipelining the processor adds 0.2ns of overhead to the clock. Ignoring any latency impact, how much speed up in the instruction execution rate is achieved from this pipeline? **(04 Marks)**

PART – B

5 a. Explain with the help of appropriate pseudo statements the principle of spinlocks with EXCH synchronization primitive, highlight on its demerits. Explain the modified spinlock primitive psuedocode and its merits. **(10 Marks)**

b. Explain the meaning of the following terms used in cache controlled state transition diagram: i) Exclusive; ii) Shared and iii) invalid.
Draw the state transition diagram for:
i) Processor (C.P.U.) requests for each cache block.
ii) Bus requests for each cache block and list all the responds to the events for (i) and (ii) in tabular form. **(10 Marks)**

6 a. Explain the different compiler optimization techniques used to reduce miss rate. **(10 Marks)**

b. Explain the process of:
i) Protection via virtual memory.
ii) Protection via virtual machines. **(10 Marks)**

7 a. Explain any four memory hierarchy questions in detail. **(08 Marks)**

b. Explain the different techniques used to improve memory performance inside a DRAM chip. **(08 Marks)**

c. A parallel processing system – C is having a degree of parallelism = 10. If f = fraction of the operations performed by C and are strictly scalar (cannot be processed in parallel), speed up for the tasks under consideration = 6.5, assuming that all other operations are processed at the maximum possible rate (vector),
i) What is f?
ii) By how much f be reduced to increase the speed to 9.0? **(04 Marks)**

8 Write short notes on any Four:
a. Benchmarks.
b. Detecting and enhancing loop level parallelism.
c. Hardware support for compiler speculation.
d. Memory consistency models.
e. What makes pipelining hard to implement? **(20 Marks)**

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