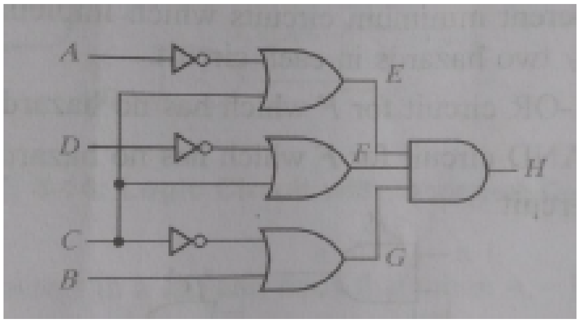
Scheme Of Evaluation
Internal Assessment Test 1 – Sept.2019

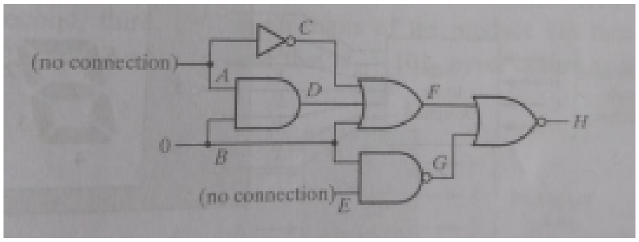
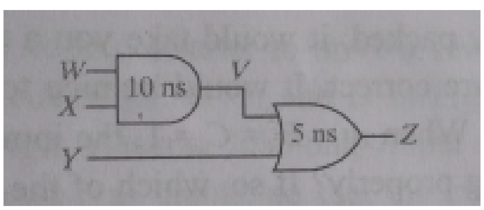
Sub:	Analog and Digital Electronics							**Code:**	18CS33
Date:	09/09/2019	**Duration:**	90mins	**Max Marks:**	50	**Sem:**	III	**Branch:**	ISE

Note: Answer Any Five Questions

Question #		Description	Marks Distribution		Max Marks
1	a)	Find the minimum SOP and the minimum POS for each function: F(a, b, c, d) = Π M (0, 1, 6, 8, 11, 12) • Using K-Map for SOP form, calculate minimum SOP • Using K-Map for POS form, calculate minimum POS	2.5M x 2	5M	10 M
	b)	F(a, b, c, d) = Σ m (1, 3, 4, 11) + Σ d (2, 7, 8, 12, 14, 15) • Using K-Map for SOP form, calculate minimum SOP • Using K-Map for POS form, calculate minimum POS	2.5M x 2	5M	
2		Find a minimum SOP solution using Quine McCluskey method F(a, b, c, d) = Σ m (2, 3, 4, 7, 9, 11, 12, 13, 14) + Σ d (1, 10, 15) • Grouping minterms based on index and Identifying prime implicants • Preparing Prime Implicant chart • Identifying Essential PI • Obtaining a minimum solution	4M 2M 2M 2M	10M	10 M
3		Find all minimum SOP solutions for the function using Petrick's method F(a, b, c, d) = Σ m (0, 3, 4, 5, 7, 9, 11, 13) • Grouping minterms based on index and	4M 2M 2M	10M	10 M

		Identifying PI and preparing PI chart • Eliminating Essential PI and its corresponding minterms and obtaining logic function P in terms of rows P1, P2, etc in PI chart • Solving for P using Boolean theorems • Identifying all possible minimum solutions for given function from solution of P.	2M		
4	a)	Using the method of map-entered variables, use 4-variable maps to find a minimum SOP expression for: $F(A, B, C, D, E) = \Sigma m(0, 4, 6, 13, 14) + \Sigma d(2, 9) + E(m_1 + m_{12})$ • K-Map for given function • K-Map for E=0 • Obtain MS0 • K-Map for E=1 • Obtain MS1 • Obtain final minimum solution	2M 2M 1M	5M	10 M
	b)	$Z(A, B, C, D, E, F, G) = \Sigma m(2, 5, 6, 9) + \Sigma d(1, 3, 4, 13, 14) + E(m_{11} + m_{12}) + Fm_{10} + Gm_0$ • K-Map for given function • K-Map for E=0, F=0, G=0 • Obtain MS0 • K-Map for E=1 • Obtain MS1 • K-Map for F=1 • Obtain MS2 • K-Map for G=1 • Obtain MS3 • Obtain final minimum solution	1M x 5	5M	
5	a)	In the circuit shown below, assume the inverters have a delay of 1 ns and the other gates have a delay of 2 ns. Initially A = B = C = 0 and D = 1; C changes to 1 at time 2 ns. Draw a timing diagram showing the glitch corresponding to the hazard. • Show timing diagrams for all inputs • Obtain timing diagrams for intermediate outputs • Obtain timing diagram for output and showing the hazard	2M x 3	6M	10 M

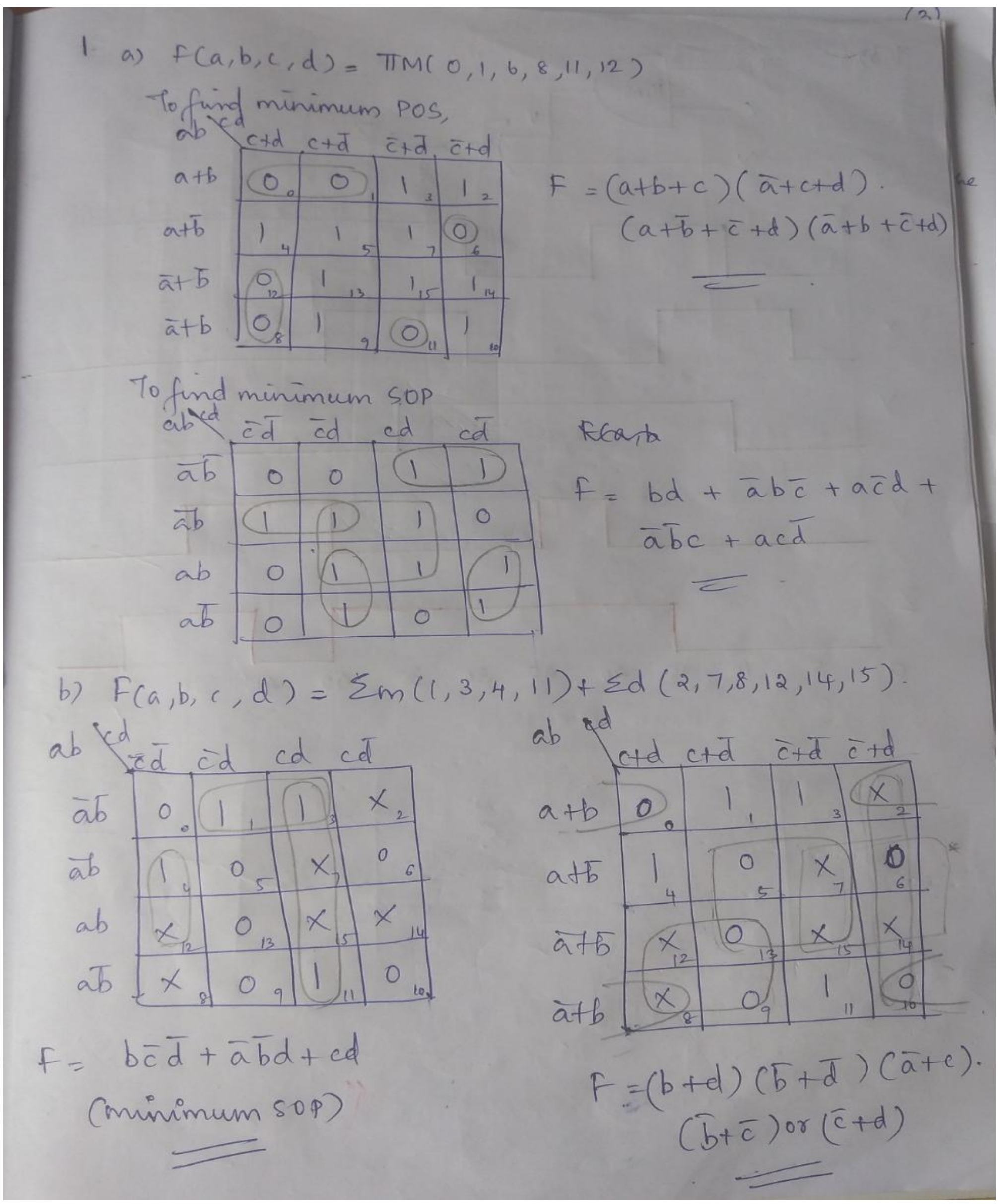
	b)	Identify the hazard as per the circuit given below. Modify the circuit so that it is hazard-free.  • Identify the type of hazard • Obtain the circuit expression with hazard • Draw the circuit with hazard and mark the hazard in it • Obtain the hazard free expression and draw the corresponding circuit diagram	1M x 4	4M	
6	a)	Show how two 2:1 multiplexers (with no added gates) could be connected to form a 3:1 MUX. Input selection should be as follows: If AB = 00, select I_0 If AB = 01, select I_1 If AB = 1- (B is a don't care), select I_2. • Show the implementation with necessary details	2M	2M	10M
	b)	Implement AND gate and OR gate using 2:1 MUX • Implement AND gate using 2:1 MUX • Implement OR gate using 2:1 MUX	2M x 2	4M	

	c)	Using four-valued logic, find A, B, C, D, E, F, G and H from the below circuit:  • Starting with A = Z and B = 0, obtain all others based on four-valued simulation logic	0.5M x 8	4M	
7	a)	What do you mean by hazards in combinational logic? What are the different types of hazards? Explain. • Description of hazards • 3 types of hazards • Description of each type with diagram/example	2M x 3	6M	10 M
	b)	Obtain the timing diagram for the circuit shown below. Assume that the AND gate has a delay of 10 ns and the OR gate has a delay of 5 ns.  • Show timing diagram of V • Show timing diagrams of Z	2M x 2	4M	
8		Write the truth table for Binary to Gray code converter and realize the same using four 8:1 multiplexers. • Binary to Gray code conversion using truth table	4M 2M 4M	10M	10 M

	• Implementation table for G3, G2, G1 and G0 • Obtain all 8 inputs to be given to each 8:1 MUX for G3, G2, G1 and G0 and implementation of four 8:1 multiplexers giving the above obtained inputs			

SOLUTIONS

1 (a)	Find the minimum SOP and the minimum POS for each function: F(a, b, c, d) = Π M (0, 1, 6, 8, 11, 12)
(b)	F(a, b, c, d) = Σ m (1, 3, 4, 11) + Σ d (2, 7, 8, 12, 14, 15)



2	Find a minimum SOP solution using Quine McCluskey method
	F(a, b, c, d) = Σ m (2, 3, 4, 7, 9, 11, 12, 13, 14) + Σ d (1, 10, 15)

2. $F(a,b,c,d) = \Sigma m(2,3,4,7,9,11,12,13,14) + \Sigma d(1,10,15)$

Column 0

1	0001 ✓
2	0010 ✓
3	0011 ✓
4	0100 ✓
7	0111 ✓
9	1001 ✓
10	1010 ✓
11	1011 ✓
12	1100 ✓
13	1101 ✓
14	1110 ✓
15	1111

Column 1

Index 1	1	0001 ✓
	2	0010 ✓
	4	0100 ✓
Index 2	3	0011 ✓
	9	1001 ✓
	10	1010 ✓
	12	1100 ✓
Index 3	7	0111 ✓
	11	1011 ✓
	13	1101 ✓
	14	1110 ✓
Index 4	15	1111 ✓

Column 2

(1,3)	00–1 ✓	
(1,9)	–001 ✓	
(2,3)	001– ✓	
(2,10)	–010 ✓	
(4,12)	–100	— I
(3,7)	0–11 ✓	
(3,11)	–011 ✓	
(9,11)	10–1 ✓	
(9,13)	1–01 ✓	
(10,11)	101– ✓	
(10,14)	1–10 ✓	
(12,13)	110– ✓	
(12,14)	11–0 ✓	
(7,15)	–111 ✓	
(11,15)	1–11 ✓	
(13,15)	11–1 ✓	
(14,15)	111– ✓	

Column 3

1,3,9,11	–0–1	II
1,9,3,11	–0–1	
2,3,10,11	–01–	III
2,10,3,11	–01–	
3,7,11,15	––11	IV
3,11,7,15	––11	
9,11,13,15	1––1	V
9,13,11,15	1––1	
10,11,14,15	1–1–	VI
10,14,11,15	1–1–	
12,13,14,15	11––	VII
12,14,13,15	11––	

PIs:

4,12	–100	$B\bar{C}\bar{D}$
1,3,9,11	–0–1	$\bar{B}D$
2,3,10,11	–01–	$\bar{B}C$
3,7,11,15	––11	CD
9,11,13,15	1––1	AD
10,11,14,15	1–1–	AC
12,13,14,15	11––	AB

PI chart.

PIs	m_2	m_3	m_4	m_7	m_9	m_{11}	m_{12}	m_{13}	m_{14}
$B\bar{C}\bar{D}$ 4, 12			⊗				×		
$\bar{B}D$ 1, 3, 9, 11		×			×	×			
$\bar{B}C$ 2, 3, 10, 11	⊗	×				×			
CD 3, 7, 11, 15		×		⊗		×			
AD 9, 11, 13, 15					×	×		×	
AC 10, 11, 14, 15						×			×
AB 12, 13, 14, 15							×	×	×

Essential PIs $\rightarrow B\bar{C}\bar{D}$, $\bar{B}C$, CD.

These 3 terms together cover minterms 2, 3, 4, 7, 11 & 12.
Remaining minterms to be covered are 9, 13 & 14.
∴ We should select a minimum no. of PIs that cover these 3.

1) 9 can be covered by $\bar{B}D$ or AD. We select AD as this term covers both 9 and 13.

2) Now, only 14 is left. This can be covered by AC or AB. We can chose any one of these

∴ Minimum SOP solution is

$$B\bar{C}\bar{D} + \bar{B}C + CD + AD + AC$$

or

$$B\bar{C}\bar{D} + \bar{B}C + CD + AD + AB$$

3	Find all minimum SOP solutions for the function using Petrick's method
	F(a, b, c, d) = Σ m (0, 3, 4, 5, 7, 9, 11, 13)

3. $F(a,b,c,d) = \Sigma m\,(0,3,4,5,7,9,11,13)$

Column 0

0	0000 ✓
3	0011 ✓
4	0100 ✓
5	0101 ✓
7	0111 ✓
9	1001 ✓
11	1011
13	1101

Column 1

Index 0	0	0000 ✓
Index 1	4	0100 ✓
Index 2	3	0011 ✓
	5	0101 ✓
	9	1001 ✓
Index 3	7	0111 ✓
	11	1011 ✓
	13	1101 ✓

Column 2

0,4	0–00
4,5	010–
3,7	0–11
3,11	–011
5,7	01–1
5,13	–101
9,11	10–1
9,13	1–01

All are PIs.

PIs.

0,4	0–00	$\bar{A}\bar{C}\bar{D}$
4,5	010–	$\bar{A}B\bar{C}$
3,7	0–11	$\bar{A}CD$
3,11	–011	$\bar{B}CD$
5,7	01–1	$\bar{A}BD$
5,13	–101	$B\bar{C}D$
9,11	10–1	$A\bar{B}D$
9,13	1–01	$A\bar{C}D$

PI chart

PIs	m0 ✓	m3	m4 ✓	m5	m7	m9	m11	m13	
$\bar{A}\bar{C}\bar{D}$ 0,4 EPI	X		X						
$\bar{A}B\bar{C}$ 4,5			X	X					P1
$\bar{A}CD$ 3,7		X			X				P2
$\bar{B}CD$ 3,11		X					X		P3
$\bar{A}BD$ 5,7				X	X				P4
$B\bar{C}D$ 5,13				X				X	P5
$A\bar{B}D$ 9,11						X	X		P6
$A\bar{C}D$ 9,13						X		X	P7

$\bar{A}\bar{C}\bar{D}$ is an essential PI. It covers minterms 0 and 4.

So only the remaining PIs need to be considered in Petrick's method to cover minterms 3, 5, 7, 9, 11 & 13. Naming them as $P_1, P_2 \ldots P_7$.

$$\therefore P = (P_2+P_3)(P_1+P_4+P_5)(P_2+P_4)(P_6+P_7)(P_3+P_6)(P_5+P_7)$$

$$= (P_2+P_3)(P_2+P_4) \Rightarrow P_2 + P_3P_4$$

$$(P_6+P_7)(P_6+P_3) \Rightarrow P_6 + P_3P_7$$

$$\therefore P = \cancel{(P_3+P_2P_6)(P_1+P_5P_6)(P_1+P_4+P_5)(P_2+P_4)}$$

$$(P_1+P_4+P_5)(P_5+P_7) \Rightarrow P_5 + P_1P_7 + P_4P_7$$

$$\therefore P = (P_2+P_3P_4)(P_6+P_3P_7)(P_5+P_1P_7+P_4P_7)$$

$$= (P_2P_6 + P_2P_3P_7 + P_3P_4P_6 + P_3P_4P_7)(P_5+P_1P_7+P_4P_7)$$

$$= P_2P_5P_6 + P_2P_3P_5P_7 + P_3P_4P_5P_6 + \cancel{P_3P_4P_5P_7} +$$

$$P_1P_2P_6P_7 + P_1P_2P_3P_7 + \cancel{P_1P_3P_4P_6P_7} + \cancel{P_1P_3P_4P_7} +$$

$$P_2P_4P_6P_7 + \cancel{P_2P_3P_4P_7} + \cancel{P_3P_4P_6P_7} + \underline{P_3P_4P_7}$$

$$= \underset{1}{P_2P_5P_6} + \underset{2}{P_3P_4P_7} + \underset{3}{P_2P_3P_5P_7} + \underset{4}{P_3P_4P_5P_6} +$$

$P_1P_2P_6P_7 + P_1P_2P_3P_7 + P_2P_4P_6P_7$.

(5) (6) (7) .

⇒ 7 possible solutions.

Out of these 7, (1) and (2) are minimum solutions.

i.e., $P_2P_5P_6 \rightarrow \bar{A}CD + B\bar{C}D + A\bar{B}D + \boxed{\bar{A}\bar{C}\bar{D}}$

& $P_3P_4P_7 \rightarrow \bar{B}CD + \bar{A}BD + A\bar{C}D + \boxed{\bar{A}\bar{C}\bar{D}}$

Essential Prime Implicant.

4	Using the method of map-entered variables, use 4-variable maps to find a minimum SOP expression for:
(a)	$F(A, B, C, D, E) = \Sigma\, m\,(0, 4, 6, 13, 14) + \Sigma\, d\,(2, 9) + E(m_1 + m_{12})$
(b)	$Z(A, B, C, D, E, F, G) = \Sigma\, m\,(2, 5, 6, 9) + \Sigma\, d\,(1, 3, 4, 13, 14) + E(m_{11} + m_{12}) + Fm_{10} + Gm_0$

6.24 (a) (MEV) $F(A, B, C, D, E) = \Sigma m\,(0, 4, 6, 13, 14) + \Sigma d\,(2, 9) + E\,(m_1 + m_{12})$

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1 (0)	E (1)	0 (3)	X (2)
$\bar{A}B$	1 (4)	0 (5)	0 (7)	1 (6)
AB	E (12)	1 (13)	0 (15)	1 (14)
$A\bar{B}$	0 (8)	X (9)	0 (11)	0 (10)

① When $E = 0$

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	0	X
$\bar{A}B$	1	0	0	F
AB	0	1	0	1
$A\bar{B}$	0	X	0	0

$\therefore MS_0 = \bar{A}\bar{D} + A\bar{C}D + B\bar{C}\bar{D}$

② When $E = 1$

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	X	1	0	X
$\bar{A}B$	X	0	0	X
AB	1	X	0	X
$A\bar{B}$	0	X	0	0

$\therefore MS_1 = E\bar{A}\bar{B}\bar{C} / \bar{B}\bar{C}DE +$
$AB\bar{C}\bar{E} / B\bar{C}\bar{D}\bar{E}$

$\therefore F = MS_0 + MS_1$

$= \bar{A}\bar{D} + A\bar{C}D + BC\bar{D} + (\bar{A}\bar{B}\bar{C}\bar{E} / \bar{B}\bar{C}DE) + (AB\bar{C}\bar{E} / B\bar{C}\bar{D}\bar{E})$

(b) $Z(A,B,C,D,E,F,G) = \Sigma m(2,5,6,9) + \Sigma d(1,3,4,13,14) + E(m_{11} + m_{12}) + Fm_{10} + Gm_0$

MEV 13

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	G_0	X_1	X_3	1_2
$\bar{A}B$	X_4	1_5	0_7	1_6
AB	E_{12}	X_{13}	0_{15}	X_{14}
AB	0_8	1_9	E_{11}	F_{10}

① When $E = F = G = 0$

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	x	x	1
$\bar{A}B$	x	1	0	1
AB	0	x	0	x
$A\bar{B}$	0	1	0	0

$$MS_0 = \bar{C}D + \bar{A}C\bar{D}$$

② When $E = 1,\ F = G = 0$.

0	x	x	x
x	x	0	x
1	x	0	x
0	x	1	0

$$MS_1 = \bar{B}DE + B\bar{C}E \,/\, B\bar{D}E$$

③ When $F = 1,\ E = G = 0$

0	x	x	x
x	x	0	x
0	x	0	x
0	x	0	1

$$MS_2 = C\bar{D}F$$

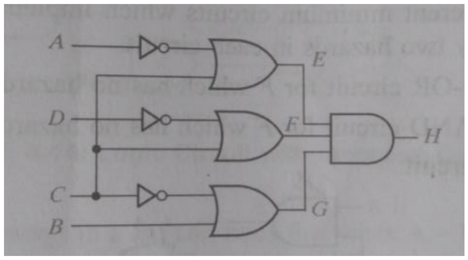
④ When $G = 1,\ E = F = 0$.

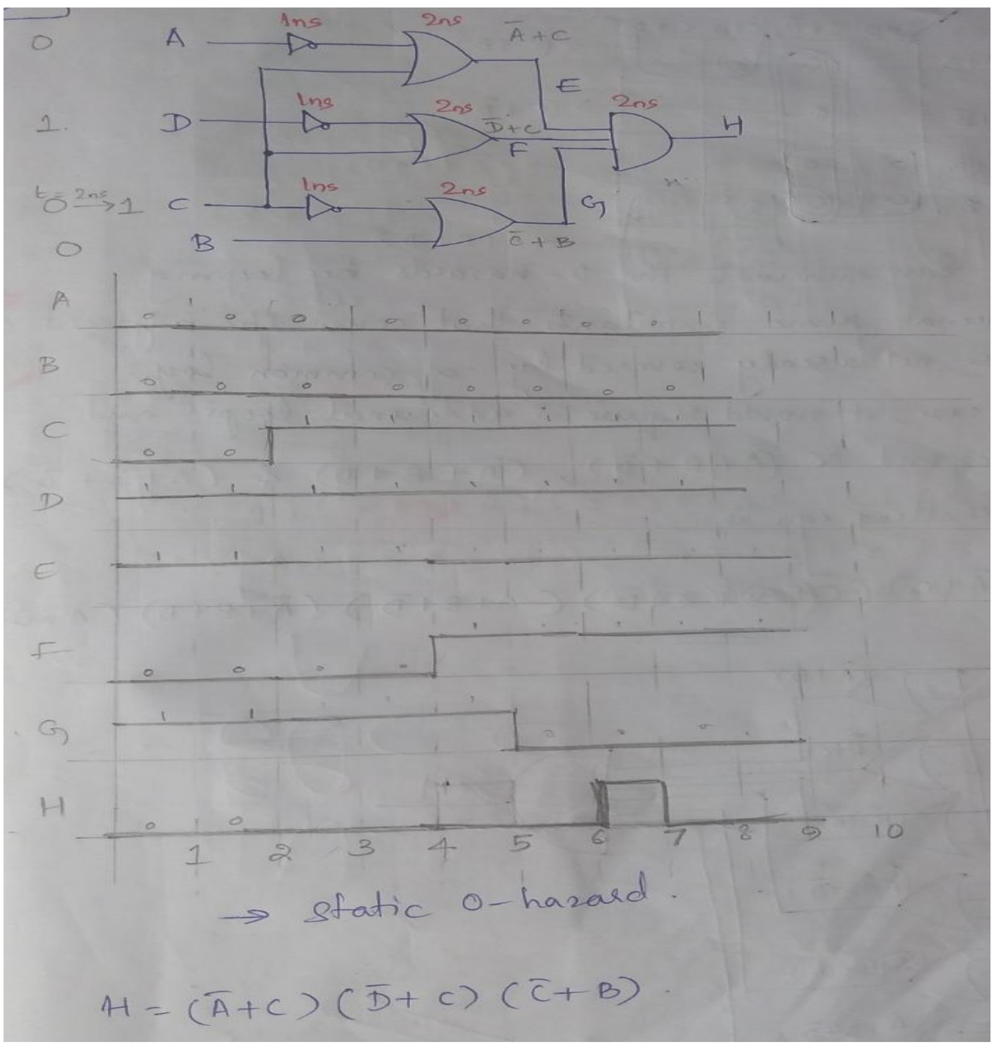
1	x	x	x
x	x	0	x
0	x	0	x
0	x	0	0

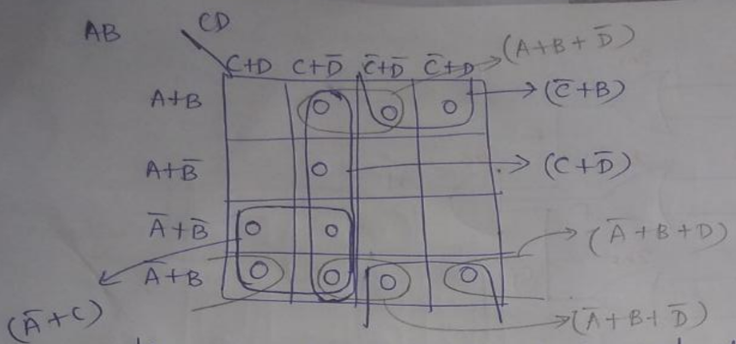
$$MS_3 = \bar{A}\bar{B}G \,/\, \bar{A}\bar{C}G \,/\, \bar{A}\bar{D}G$$

$$\therefore Z = \bar{C}D + \bar{A}C\bar{D} + \bar{B}DE + (B\bar{C}E / B\bar{D}E) + C\bar{D}F + (\bar{A}\bar{B}G / \bar{A}\bar{C}G \,|\, \bar{A}\bar{D}G)$$

5 (a)	In the circuit shown below, assume the inverters have a delay of 1 ns and the other gates have a delay of 2 ns. Initially A = B = C = 0 and D = 1; C changes to 1 at time 2 ns. Draw a timing diagram showing the glitch corresponding to the hazard.
(b)	Identify the hazard as per the circuit given below. Modify the circuit so that it is hazard-free.



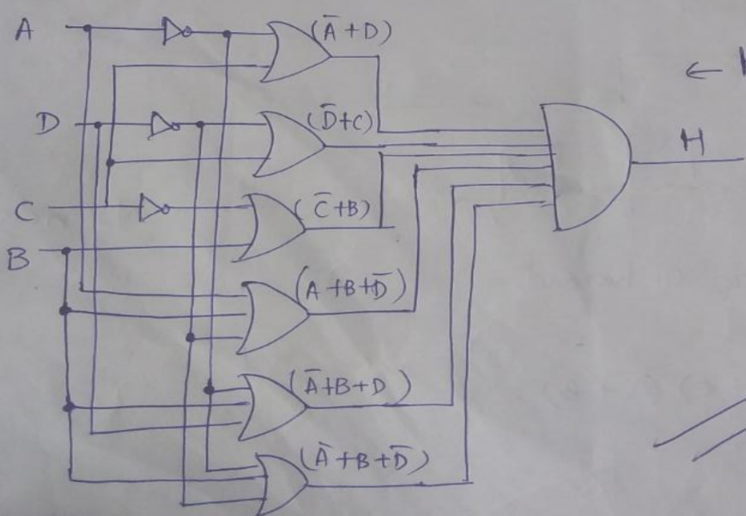




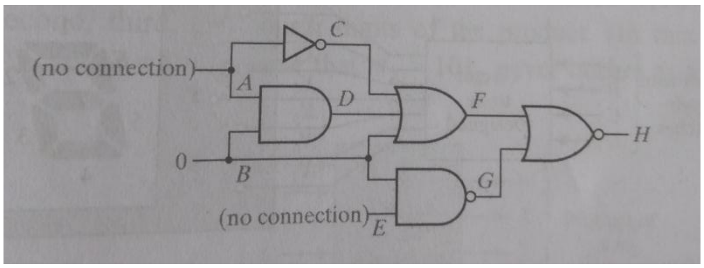
We can eliminate the 0-hazards by looping additional prime implicants that cover the adjacent 0s that are not already covered by a common loop.
In this case, it would require 3 additional loops and they correspond to $(A+B+\bar{D})$, $(\bar{A}+B+D)$ & $(\bar{A}+B+\bar{D})$

$\therefore$ The resulting eqn is:

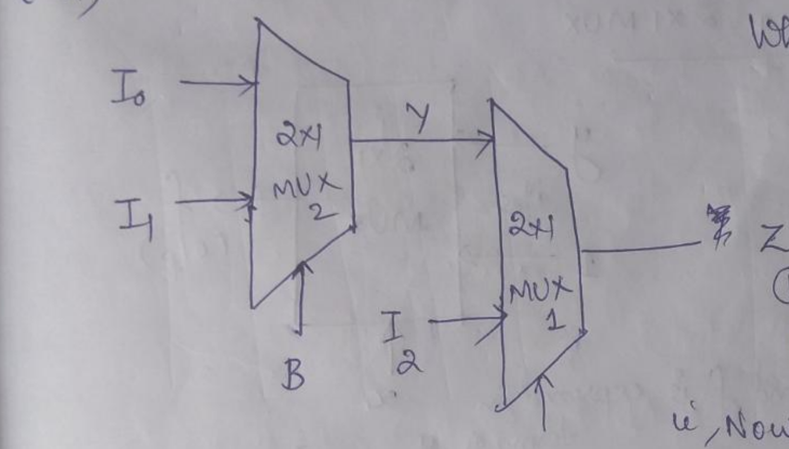
$$H = (\bar{A}+C)(\bar{C}+B)(C+\bar{D})(A+B+\bar{D})(\bar{A}+B+D)(\bar{A}+B+$$



← Hazardfree circuit

6 (a)	Show how two 2:1 multiplexers (with no added gates) could be connected to form a 3:1 MUX. Input selection should be as follows: If AB = 00, select I_0 If AB = 01, select I_1 If AB = 1- (B is a don't care), select I_2.
(b)	Implement AND gate and OR gate using 2:1 MUX
(c)	Using four-valued logic, find A, B, C, D, E, F, G and H from the below circuit: 

6. a)



When A = 0, 1st i/p (i.e, Y) of MUX 1 will be routed to o/p, Z.
Y in turn depends on value of B.

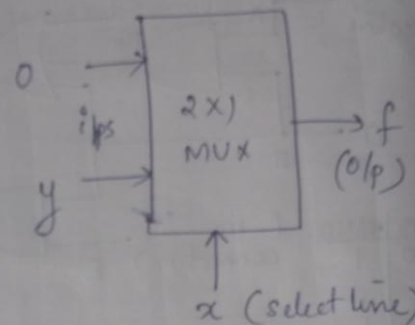
① Now, if B = 0, I_0 will be routed through Y to Z.
i.e, Now AB = 00, so Z = I_0.

② If B = 1, I_1 will be routed through Y to Z. ∴ AB = 01, so Z = I_1.

③ If A = 1, 2nd i/p of MUX 1, i.e, I_2 will be routed to Z.
i.e, AB = 1–, ∴ Z = I_2

6.b). AND gate using 2:1 MUX

x	y	f
0	0	0
0	1	0
1	0	0
1	1	1



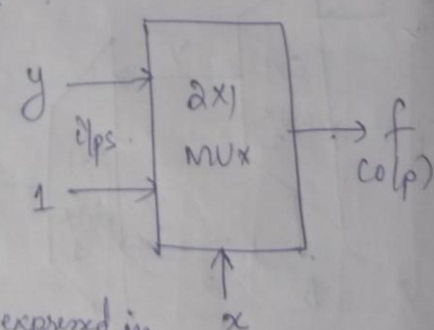
Here, we have expressed o/p of AND gate (f) in terms of i/p y.

If select line x is 0, f is independent of y, and f is always 0. So 1st i/p to MUX is 0.

If select line x is 1, f is same as y. So 2nd i/p to MUX is y.

OR gate using 2×1 MUX

x	y	f
0	0	0
0	1	1
1	0	1
1	1	1

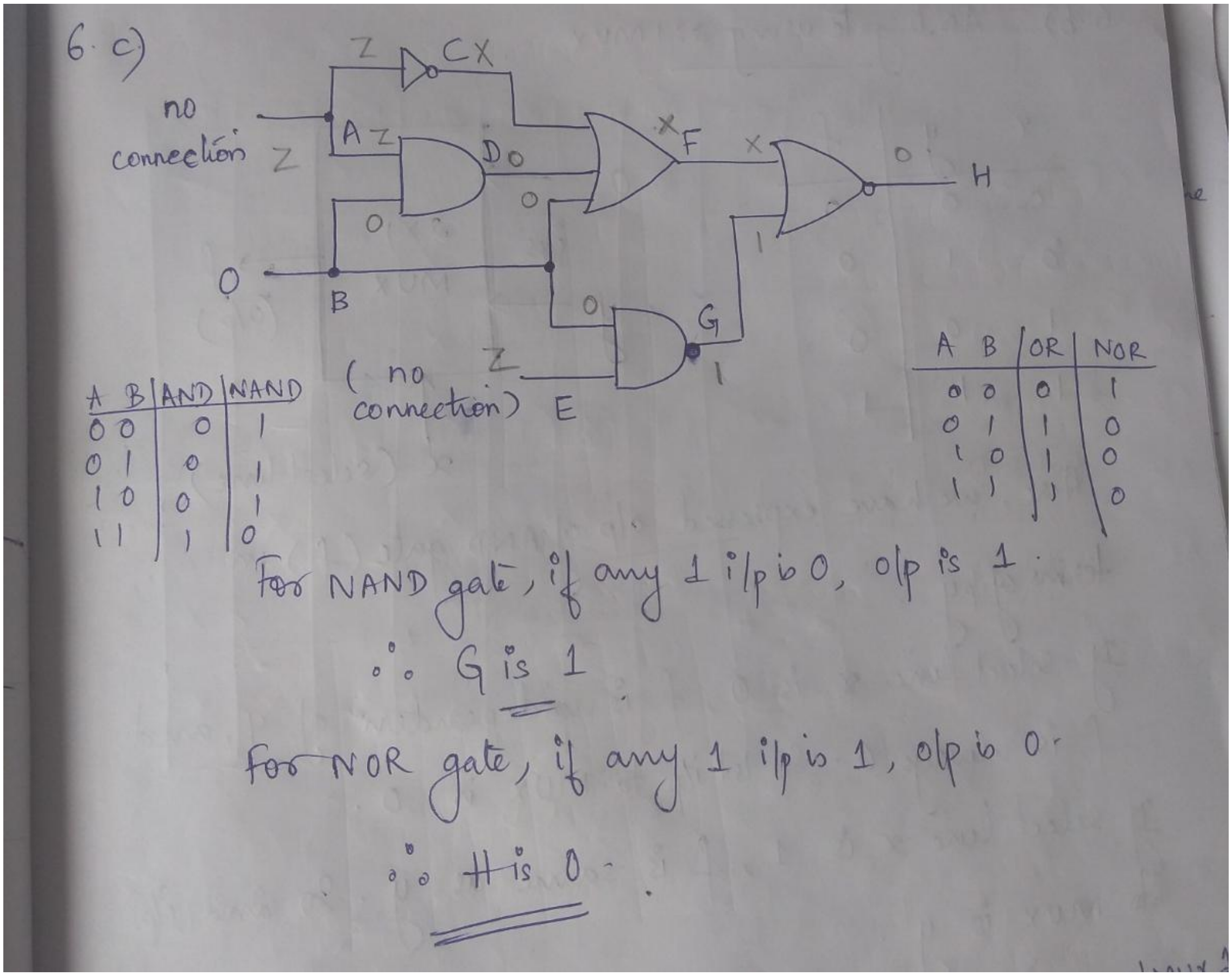


x is the select line and f is expressed in terms of y.

When x = 0, f = y. So 1st i/p to MUX is y.

When x = 1, f = 1 irrespective of y. ∴ 2nd i/p to MUX is 1

6. c)



A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

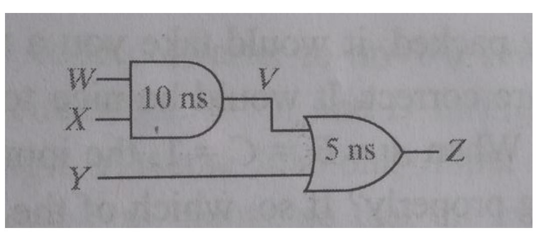
A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

For NAND gate, if any 1 i/p is 0, o/p is 1.

∴ G is 1

For NOR gate, if any 1 i/p is 1, o/p is 0.

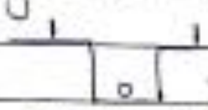
∴ H is 0.

7 (a)	What do you mean by hazards in combinational logic? What are the different types of hazards? Explain.
(b)	Obtain the timing diagram for the circuit shown below. Assume that the AND gate has a delay of 10 ns and the OR gate has a delay of 5 ns. 

Ans: When the input to a combinational circuit changes, unwanted switching transients may appear in the output. These transient occurs when different paths from input to output have different propagation delays. This leads to Hazards in combinational logic.

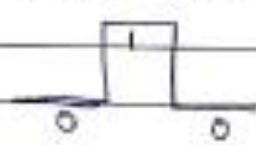
Different types of Hazards are
① Static 1 Hazard
② Static 0 Hazard
③ Dynamic Hazard.

Static 1 Hazard:
① If, in response to any single input change and for combination of propagation delays, a circuit output may momentarily go to 0 when it should remain a constant 1. Then we say that circuit has a static 1 hazard.



Static 1 Hazard.

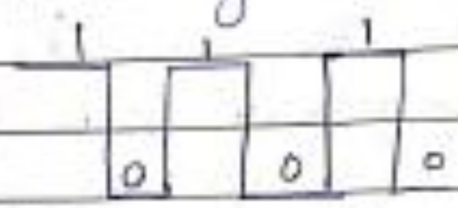
② Static 0 Hazard:
If the output may momentarily go to 1 when it should remain a 0, we say that the circuit has a static 0 Hazard.



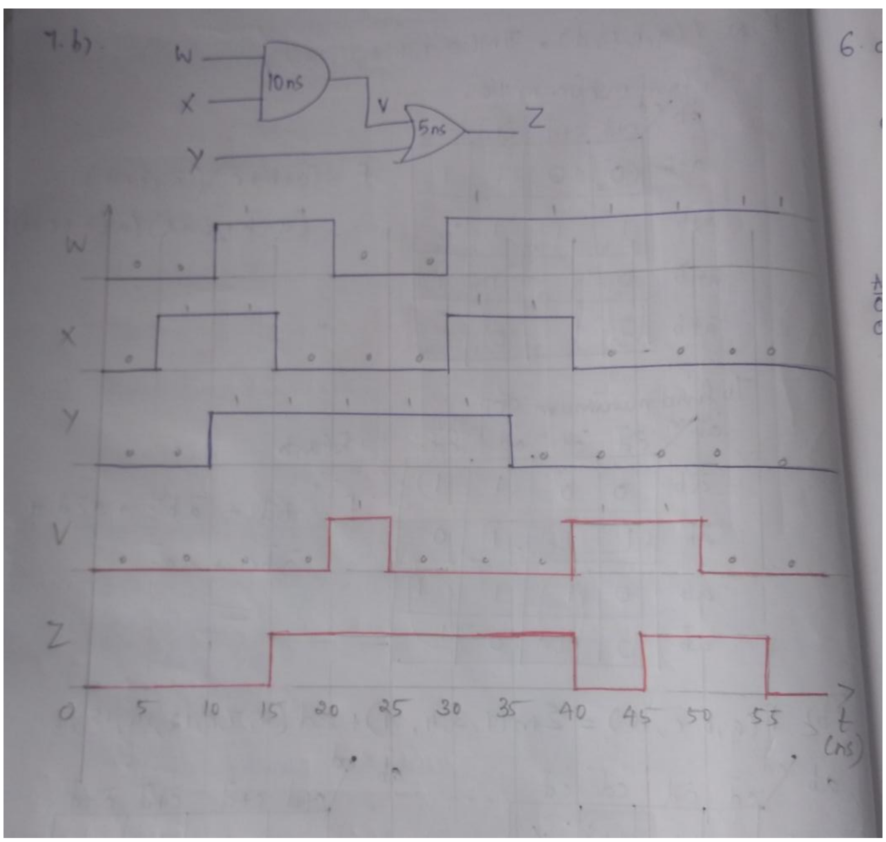
Static 0 Hazard.

③ Dynamic Hazard:

If, when the output is supposed to change from 0 to 1 or 1 to 0, the output may change three or more times. Then we say that the circuit has a dynamic Hazard.



Dynamic Hazard.

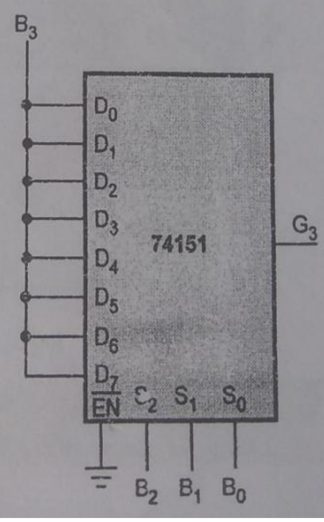


8	Write the truth table for Binary to Gray code converter and realize the same using four 8:1 multiplexers.

Binary				Gray			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

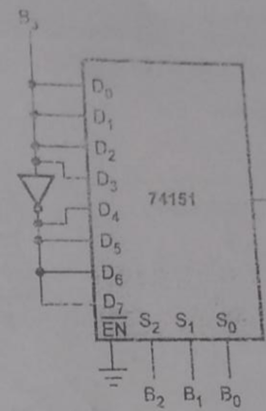
Implementation table for G_3 :

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\overline{B_3}$	0	0	0	0	0	0	0	0
B_3	1	1	1	1	1	1	1	1
	B_3	B_3	B_3	B_3	B_3	B_3	B_3	B_3



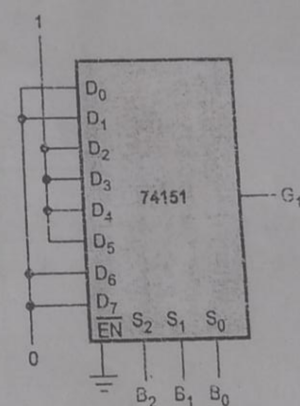
Implementation table for G_2 :

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\overline{B}_3$	0	0	0	0	1	1	1	1
B_3	1	1	1	1	0	0	0	0
	B_3	B_3	B_3	B_3	$\overline{B}_3$	$\overline{B}_3$	$\overline{B}_3$	$\overline{B}_3$



Implementation table for G_1 :

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\overline{B}_3$	0	0	1	1	1	1	0	0
B_3	0	0	1	1	1	1	0	0
	0	0	1	1	1	1	0	0



Implementation table for G_0 :

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\overline{B}_3$	0	1	1	0	0	1	1	0
B_3	0	1	1	0	0	1	1	0
	0	1	1	0	0	1	1	0