Internal Assessment Test 1 – Sep-2019									
Sub:	Analog and Digital Electronics					Sub Code:	18CS33	Branch:	CSE
Date:	09/09/19	Duration:	90 mins	Max Marks:	50	Sem/ Sec:	3rd /A,B,C		OBE

Answer any FIVE FULL Questions	MARKS	CO	RBT
1.	[2+4]	CO3	L1,L3

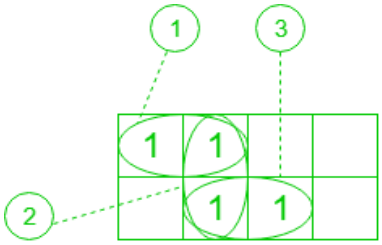
i.Define

1. **Implicants**
2. **Prime Implicants**
3. **Essential Prime implicants**
4. **Selective prime implicants**

Answer:

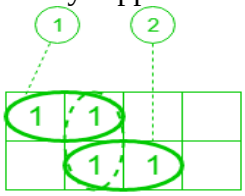
1. **Implicants:**
   Implicant is a product/minterm term in Sum of Products (SOP) or sum/maxterm term in Product of Sums (POS) of a Boolean function. E.g., consider a boolean function, F = AB + ABC + BC. Implicants are AB, ABC and BC.

2. **Prime Implicants:**
   A group of square or rectangle made up of bunch of adjacent minterms which is allowed by definition of K-Map are called **prime implicants(PI)** i.e. all possible groups formed in K-Map.



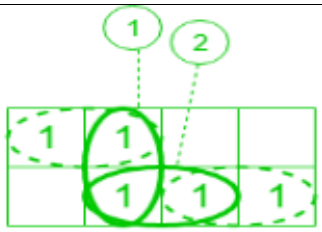
No. of Prime Implicants = 3

3. **Essential Prime Implicants**
   These are those subcubes(groups) which cover atleast one minterm that can't be covered by any other prime implicant. **Essential prime implicants (EPI)** are those prime implicants which always appear in final solution.



No. of Essential Prime Implicants = 2

4. **SelectivePrimeImplicants**
   The prime implicants for which are neither essential nor redundant prime implicants are called **selective prime implicants(SPI)**. These are also known as non-essential prime implicants. They may appear in some solution or may not appear in some solution.



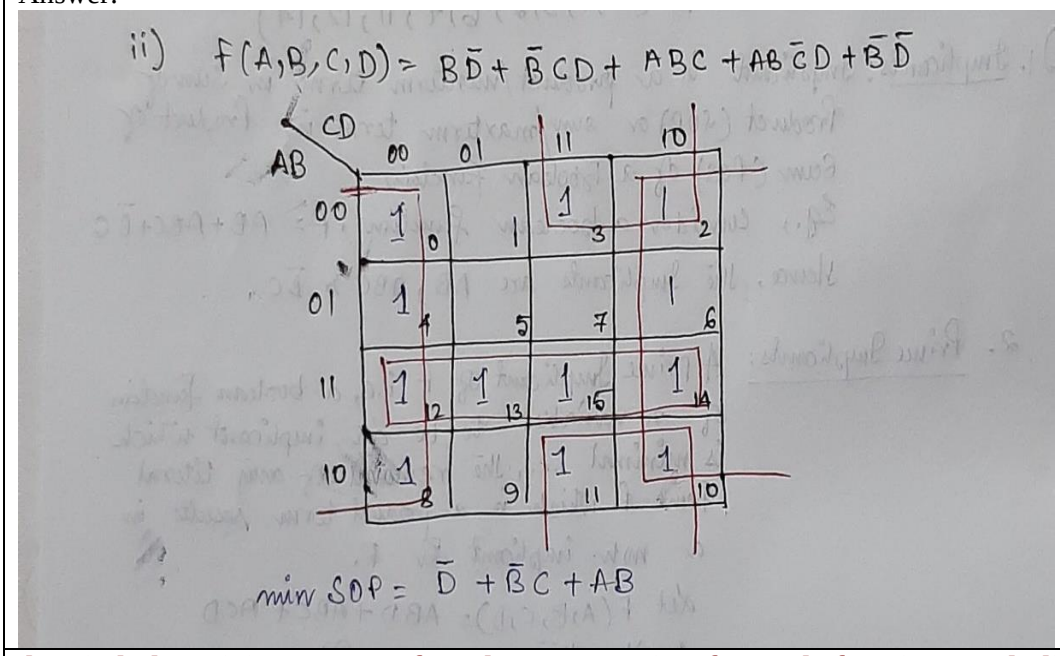
No. of Selective Prime Implicants = 2

ii. Plot the following function on a Karnaugh map. (Do not expand to min term form before plotting.)

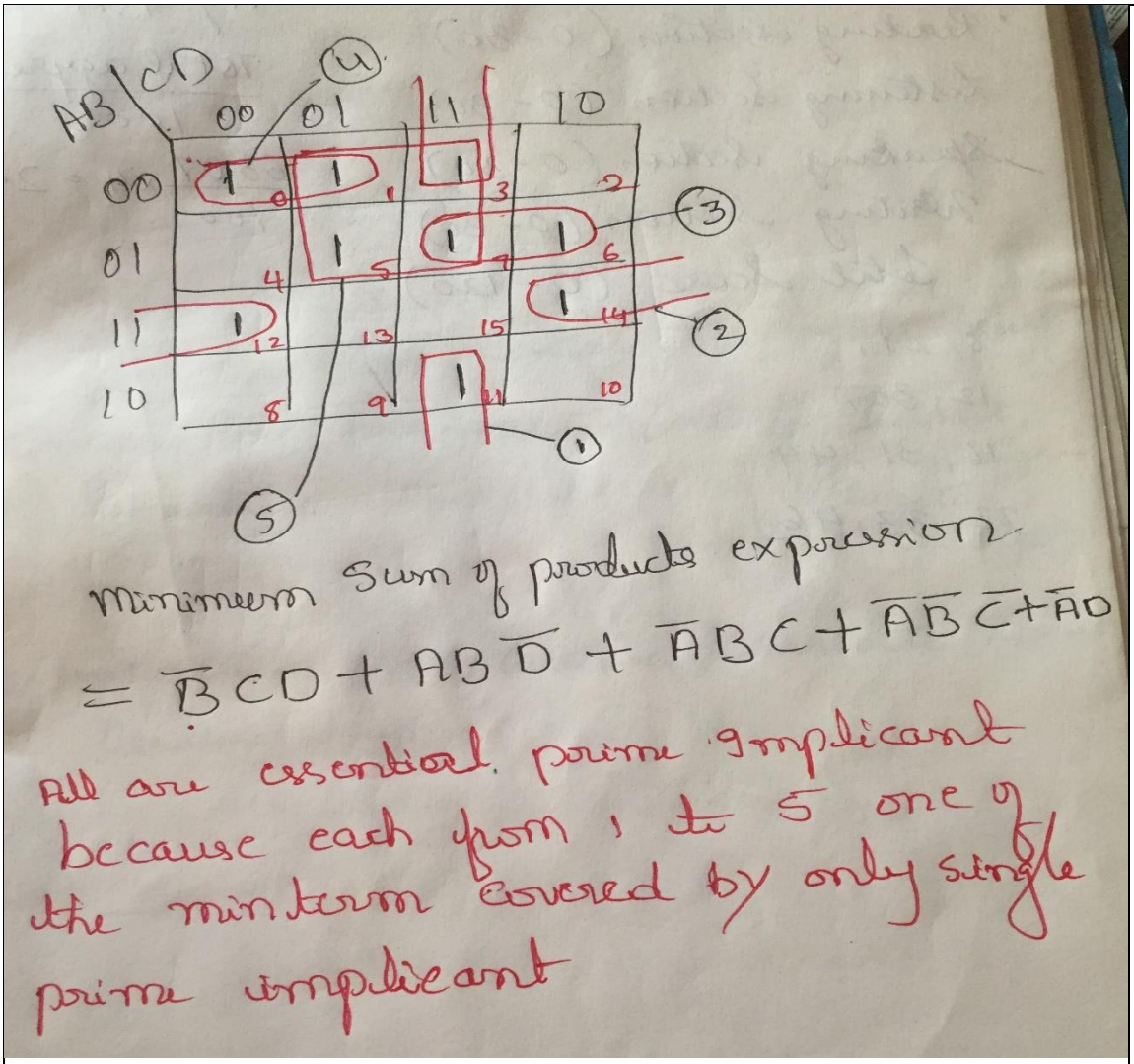
F(A,B,C,D) = BD' + B'CD +ABC +ABC'D +B'D'

Find the minimum sum of products.

Answer:



1.b. Find the minimum sum-of-products expression for each function. Underline the essential prime implicants in your answer and tell which min term makes each one essential. ***f* (*A*,*B*,*C*,*D*) = *m*(0, 1, 3, 5, 6, 7, 11, 12, 14)** **Answer:**	[4]	CO3	L3



2	[10]	CO3	L3

2. A switching circuit has two control inputs (*C*1 and *C*2), two data inputs (*X*1 and *X*2),and one output (*Z*).The circuit performs logic operations on the two data inputs, as shown in this table:

C1	C2	Function
0	0	X1X2
0	1	X1⊕X2
1	0	X1+X2
1	1	X1=X2

i. Derive a truth table for *Z*.

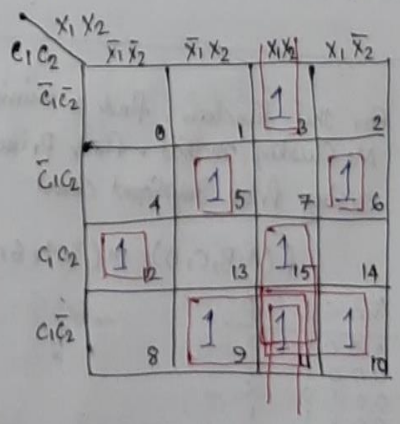
ii. Use a Karnaugh map to find a minimum OR-AND gate circuit to realize *Z*.

Answer:

Ans:

	C_1	C_2	X_1	X_2	Z	
0	0	0	0	0	0	$X_1 \cdot X_2$
1	0	0	0	1	0	
2	0	0	1	0	0	
3	0	0	1	1	1	
4	0	1	0	0	0	$X_1 \oplus X_2$
5	0	1	0	1	1	
6	0	1	1	0	1	
7	0	1	1	1	0	
8	1	0	0	0	0	$X_1 + X_2$
9	1	0	0	1	1	
10	1	0	1	0	1	
11	1	0	1	1	1	
12	1	1	0	0	1	$X_1 = X_2$
13	1	1	0	1	0	
14	1	1	1	0	0	
15	1	1	1	1	1	

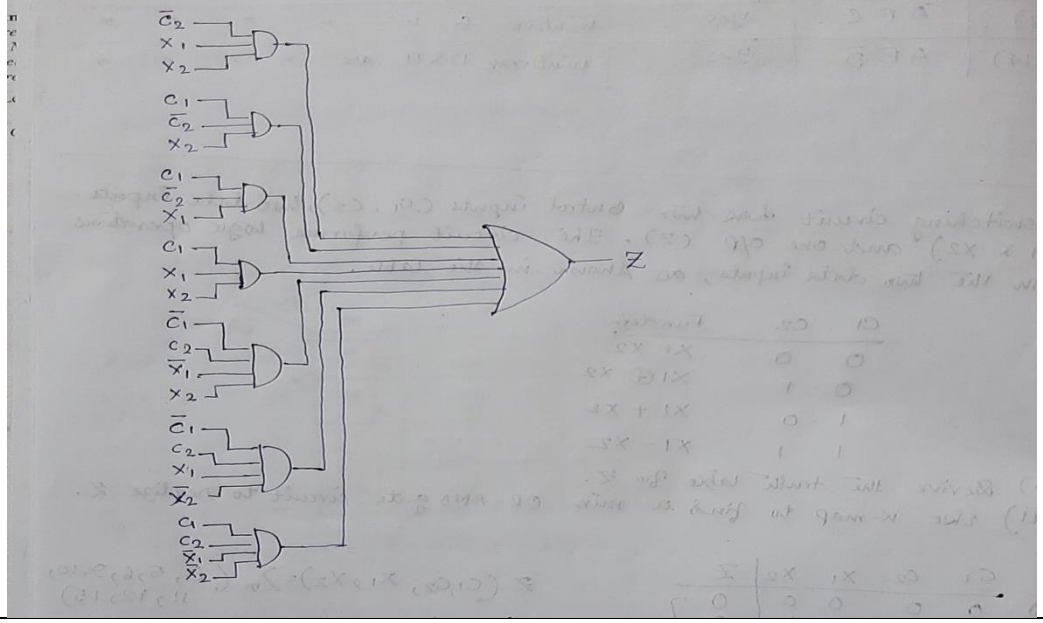
$Z(C_1, C_2, X_1, X_2) = \sum_m (3, 5, 6, 9, 10, 11, 12, 15)$



$Z(C_1, C_2, X_1, X_2)$
$= \bar{C}_2 X_1 X_2 + C_1 \bar{C}_2 X_2 + C_1 \bar{C}_2 X_1 + C_1 X_1 X_2 + \bar{C}_1 C_2 \bar{X}_1 X_2 + \bar{C}_1 C_2 X_1 \bar{X}_2 + C_1 C_2 \bar{X}_1 \bar{X}_2$

Circuit Realization Using AND-OR logic.

$Z(C_1, C_2, X_1, X_2) = \bar{C}_2 X_1 X_2 + C_1 \bar{C}_2 X_2 + C_1 \bar{C}_2 X_1 + C_1 X_1 X_2 + \bar{C}_1 C_2 \bar{X}_1 X_2 + \bar{C}_1 C_2 X_1 \bar{X}_2 + C_1 C_2 \bar{X}_1 \bar{X}_2$



3. **For this function, find a minimum sum-of-products solution, using the Quine-McCluskeymethod. Find prime implicant and essential prime implicant using prime implicant chart.** ***f*(*A*,*B*,*C*,*D*) = *m*(3, 4, 6, 7, 8, 9, 11, 13, 14) +*d*(2, 5, 15)** Answer:	[10]	CO3	L3

Decimal Equivalent	A	B	C	D	F
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	X
3	0	0	1	1	**1**
4	0	1	0	0	**1**
5	0	1	0	1	X
6	0	1	1	0	**1**
7	0	1	1	1	**1**
8	1	0	0	0	**1**
9	1	0	0	1	**1**
10	1	0	1	0	0
11	1	0	1	1	**1**
12	1	1	0	0	0
13	1	1	0	1	**1**
14	1	1	1	0	**1**
15	1	1	1	1	X

Input

0	
1	m4 0100 m8 1000 d2 0010
2	m3 0011 m6 0110 m9 1001 d5 0101
3	m7 0111 m11 1011 m13 1101 m14 1110
4	d15 1111

First Comparasion

0	
1	(6 , 4) 01-0 (5 , 4) 010- (9 , 8) 100- (3 , 2) 001- (6 , 2) 0-10
2	(7 , 3) 0-11 (11 , 3) -011 (7 , 6) 011- (14 , 6) -110 (11 , 9) 10-1 (13 , 9) 1-01 (7 , 5) 01-1 (13 , 5) -101
3	(15 , 7) -111 (15 , 11) 1-11 (15 , 13) 11-1 (15 , 14) 111-

Second Comparasion

0	
1	(7 , 5 , 6 , 4) 01-- (7 , 6 , 3 , 2) 0-1-
2	(15 , 11 , 7 , 3) --11 (15 , 14 , 7 , 6) -11- (15 , 13 , 11 , 9) 1--1 (15 , 13 , 7 , 5) -1-1

Prime Implicants

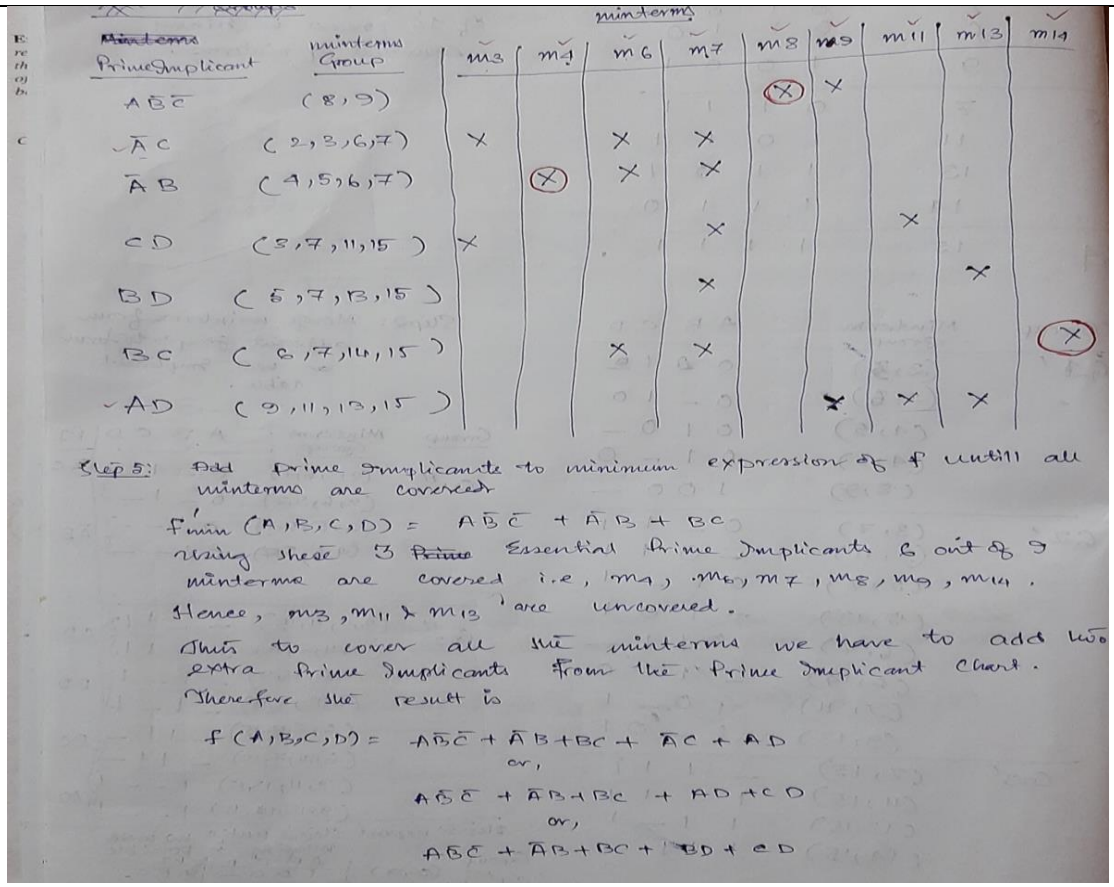
(7 , 5 , 6 , 4) 01--
(7 , 6 , 3 , 2) 0-1-
(15 , 11 , 7 , 3) --11
(15 , 14 , 7 , 6) -11-
(15 , 13 , 11 , 9) 1--1
(15 , 13 , 7 , 5) -1-1

(9 , 8) 100-

Coverage Table

	01--	0-1-	--11	-11-	1--1	-1-1	100-
3		X	X				
4	x						
6	X	X		X			
7	X	X	X	X		X	
8							x
9					X		X
11			X		X		
13					X	X	
14				x			

Prime implicant chart.



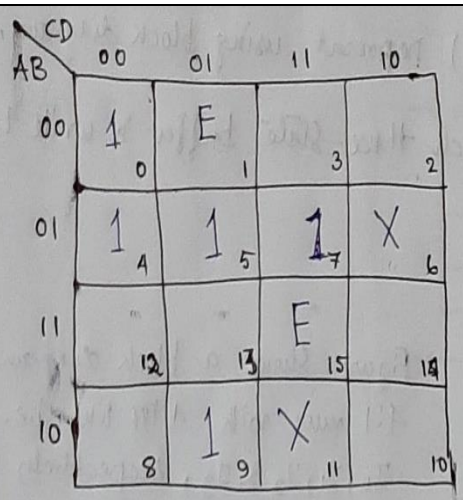
	[10]	CO3	L3

4. **Using the method of map-entered variables, use four-variable maps to find a minimum sum-of-products expression for *F*(*A*, *B*, *C*, *D*, *E*) =*m*(0, 4, 5, 7, 9) + *d*(6, 11) + E(*m*1,*m*15), where the *m*'s represent minterms of the variables *A*, *B*, *C*, and *D*.**

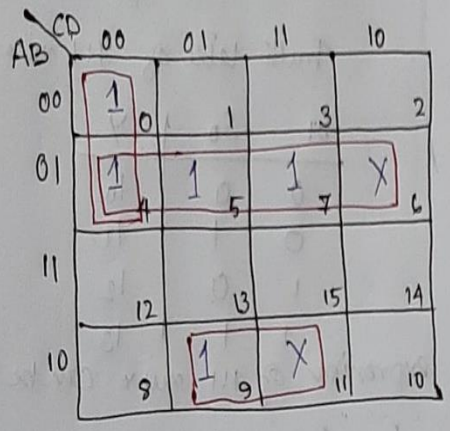
Answer:

Decimal Equivalent	A	B	C	D	F
0	0	0	0	0	1
1	0	0	0	1	0(E)
2	0	0	1	0	0
3	0	0	1	1	**0**
4	0	1	0	0	**1**
5	0	1	0	1	1
6	0	1	1	0	**X**
7	0	1	1	1	**1**
8	1	0	0	0	**0**
9	1	0	0	1	**1**
10	1	0	1	0	0
11	1	0	1	1	**X**
12	1	1	0	0	0
13	1	1	0	1	**0**
14	1	1	1	0	**0**
15	1	1	1	1	0(E)

Ans:

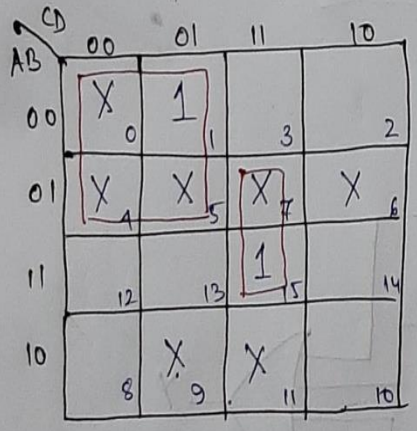


Step 1: Consider E=0 so that $F(A,B,C,D) = 1 \forall \sum m(0,4,5,7,9) + d(6,11)$



$F'(A,B,C,D) = \bar{A}B + \bar{A}\bar{C}\bar{D} + A\bar{B}D$

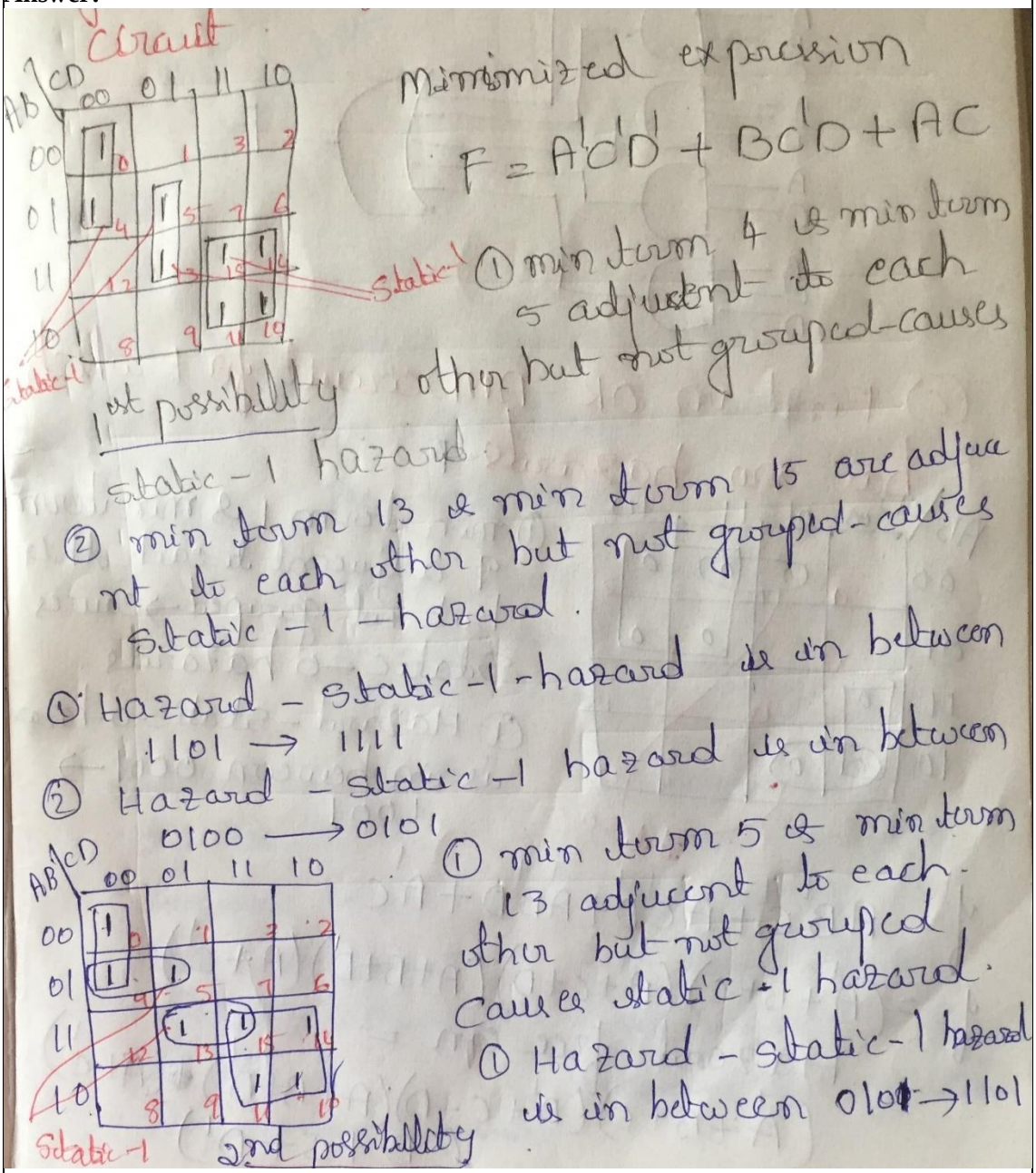
Step 2: Consider function f for variable E. Now E = 1 when $F(A,B,C,D) = 1$, considering all minterms as don't care.



$F''(A,B,C,D) = \bar{A}\bar{C}\bar{E} + BCDE$

Final Expression of minimum SOP

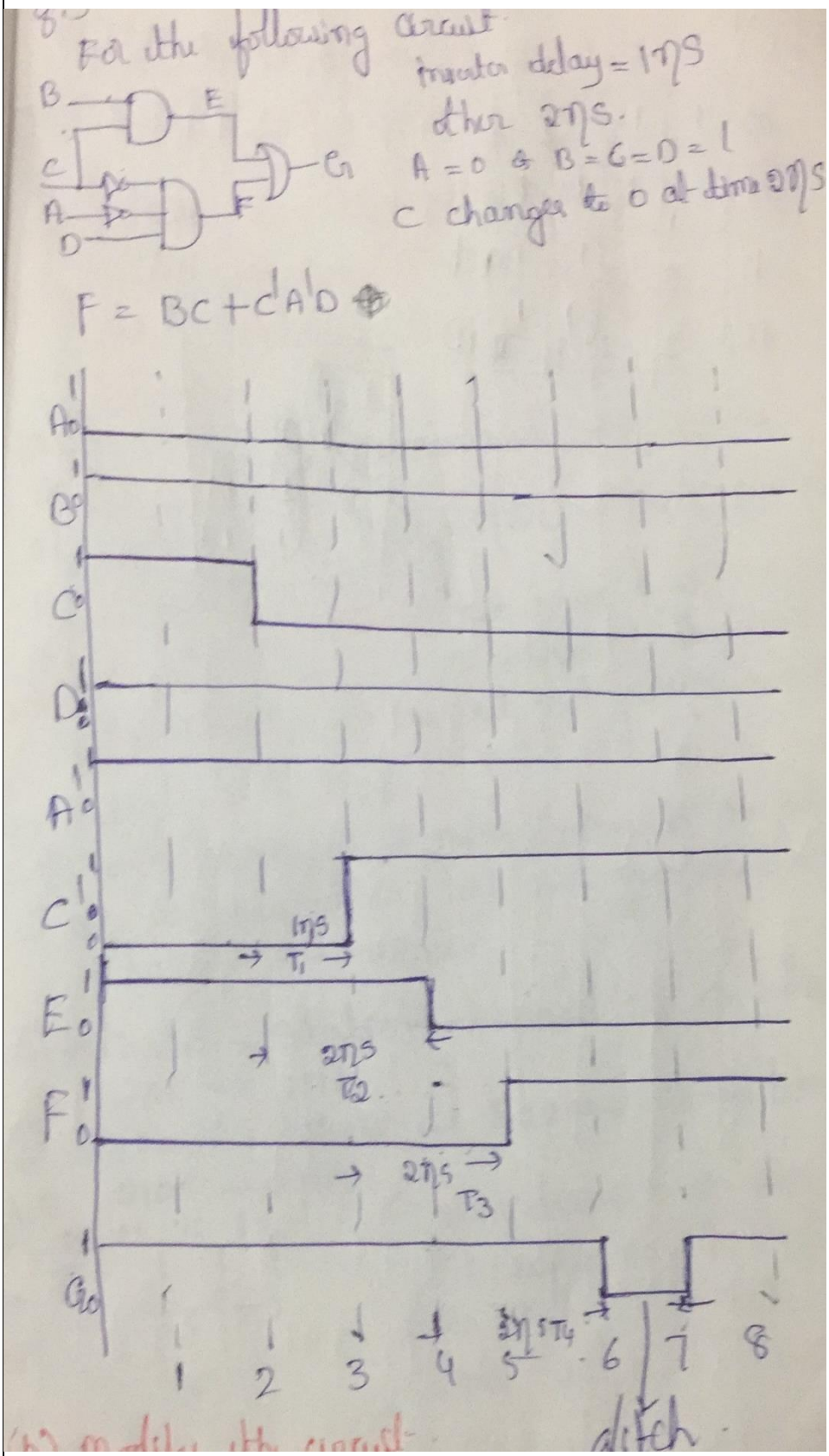
$F(A,B,C,D) = \bar{A}B + \bar{A}\bar{C}\bar{D} + A\bar{B}D + \bar{A}\bar{C}\bar{E} + BCD\bar{E}$

5a) **i..Define 1. Propagation delay 2. Hazards 3. Static -0 hazards 4. Static -1 hazards** **Answer:** 1. **Propagation Delay:-**Propagation delay, symbolized t_{pd}, is the time required for a digital signal to travel from the input(s) of a logic gate to the output 2. **Hazards:** a hazard in a digital circuit is a temporary disturbance in ideal operation of the circuit which if given some time, gets resolved itself. 3. **Static-0 Hazard:** If the output is currently at logic state 0 and after the input changes its state, the output momentarily changes to 1 before settling on 0, then it is a Static-0 hazard. 4. **Static-1 Hazard:** If the output is currently at logic state 1 and after the input changes its state, the output momentarily changes to 0 before settling on 1, then it is a Static-1 hazard. **ii.Consider the following logic function.** ***F*(*A*, *B*, *C*, *D*)= *m*(0, 4, 5, 10, 11, 13, 14, 15)** 1. **Find two different minimum circuits which implement *F* using AND and OR gates.** 2. **Identify two hazards in each circuit** **Answer:**  	**4+6**	CO4	L1 ,L3

6. **i. What is the use of simulation software? For the following circuit, Assume that the inverters have a delay of 1 ns and the other gates have a delay of 2 ns. Initially *A* =0 and *B*=*C*=*D* =1, and *C* changes to 0 at time =2 ns. Draw a timing diagram and identify the transient that occurs.**	[6+4]	CO4	L3

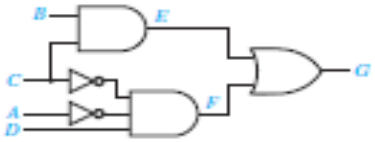
Answer:

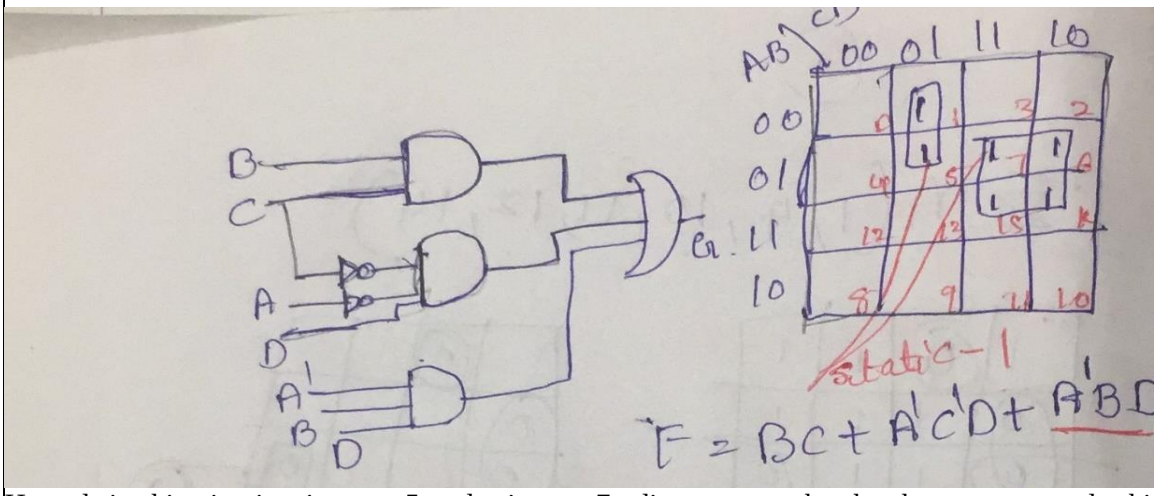
Logic simulation and circuit **simulation** are typically used in conjunction with functional verification to verify the correctness of an integrated circuit



Timing diagram

ii. Modify the circuit to eliminate the hazard.





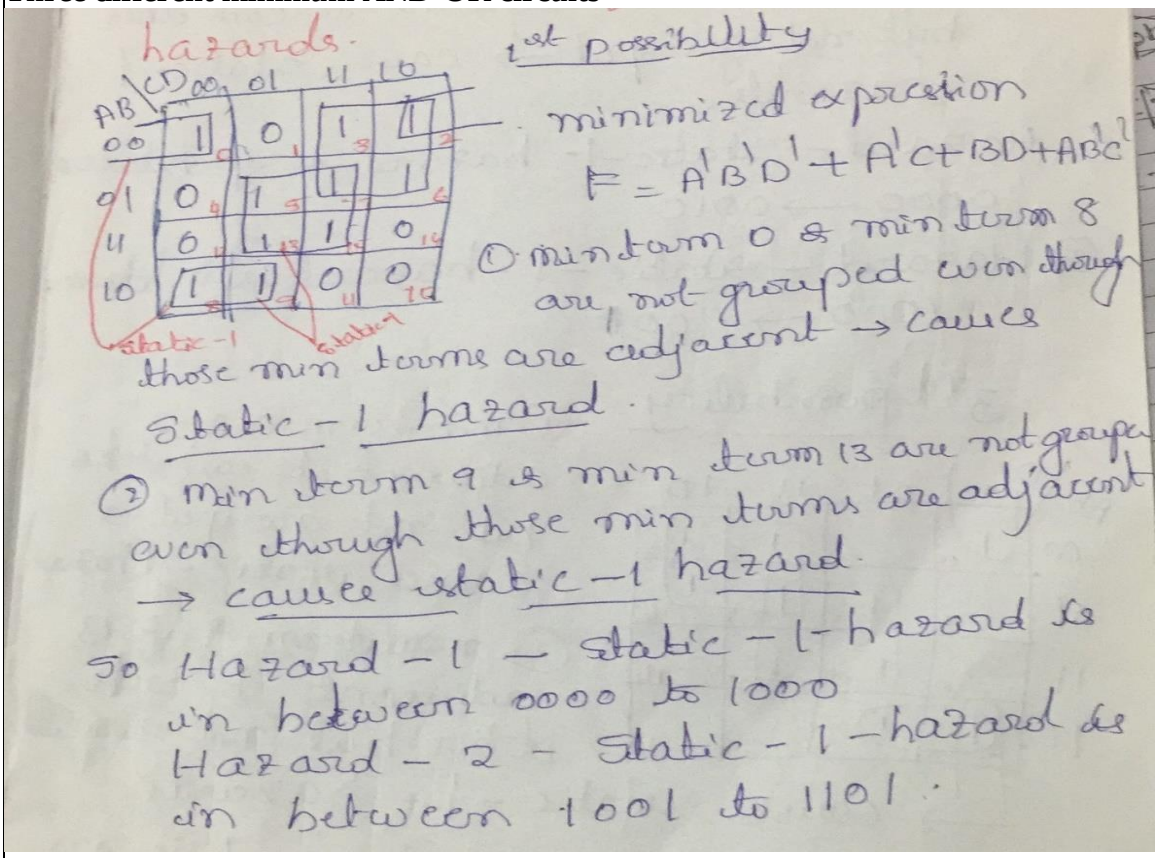
Hazard :in this circuit min term 5 and minterm 7 adjacent to each other but not grouped which causes static -1 hazard. So to this hazard eliminate by adding Min Term A'BD which eliminate the glitch.

6b. ***F*(*A, B, C, D*) =*m*(0, 2, 3, 5, 6, 7, 8, 9, 13, 15)**

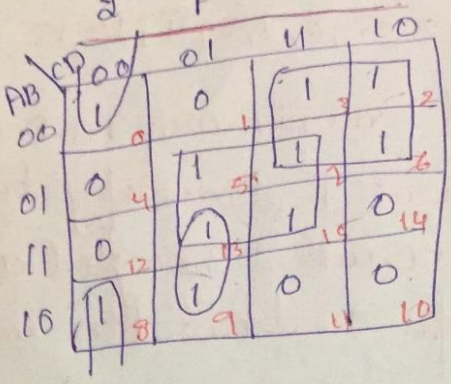
Find three different minimum AND-OR circuits that implement F.Identify two hazards in each circuit. Then find an AND-OR circuit for *F* for hazards cover

Answer:

Three different minimum AND-OR circuits



2nd possibility



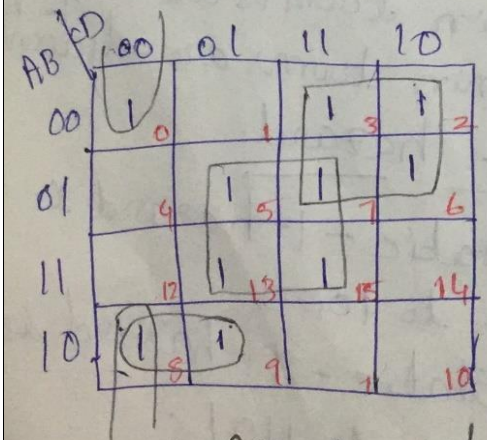
① min term 0 & 2 adjacent to each other but not grouped → causes static-1 hazards.

② min term 8 & 9 adjacent to each other but not grouped → causes static-1 hazards.

① Hazard - static-1 - hazard is in between 0000 → 0010

② Hazard - static-1 - hazard is in between 1000 → 1001

3rd possibility



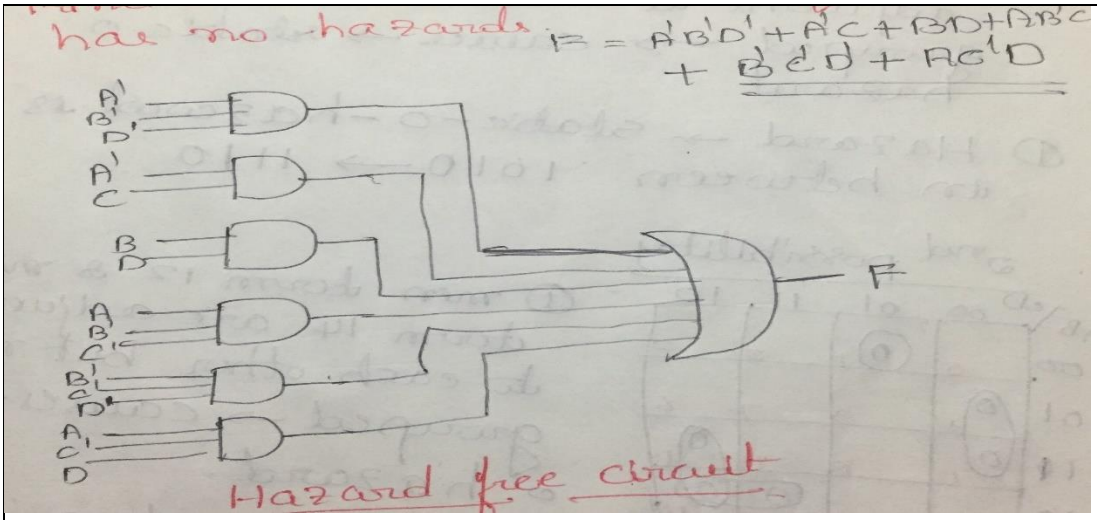
① min term 0 & 2 adjacent to each other but not grouped → causes static-1 hazards.

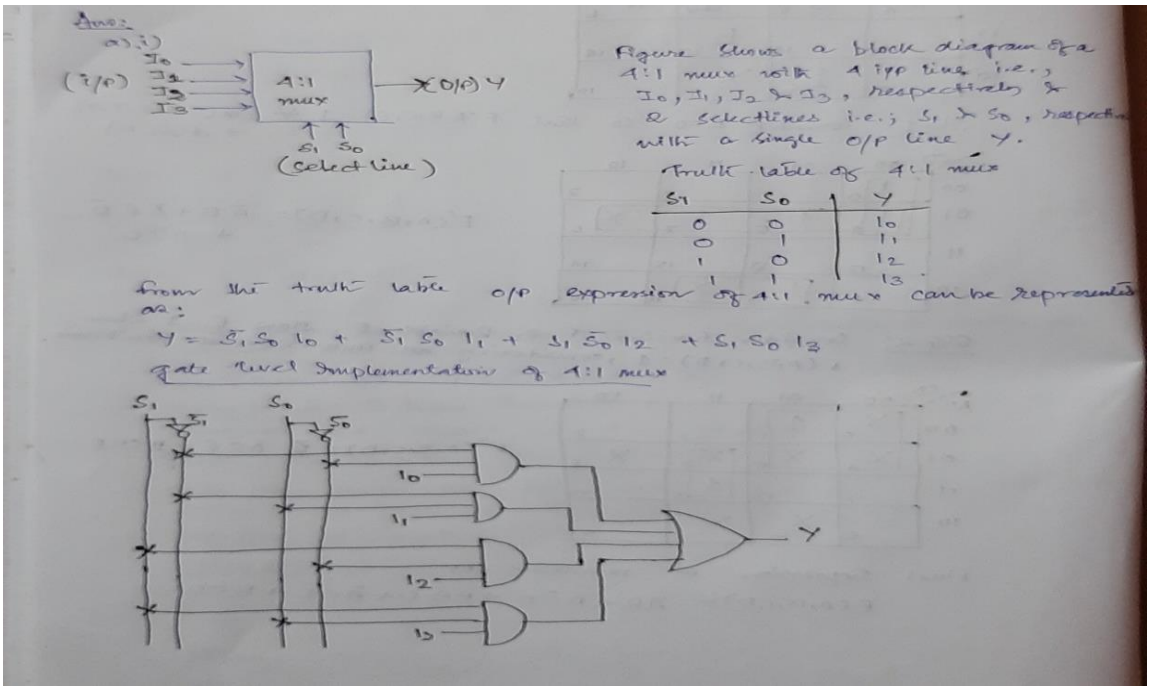
② min term 9 & 13 adjacent to each other but not grouped → causes static-1 - hazards.

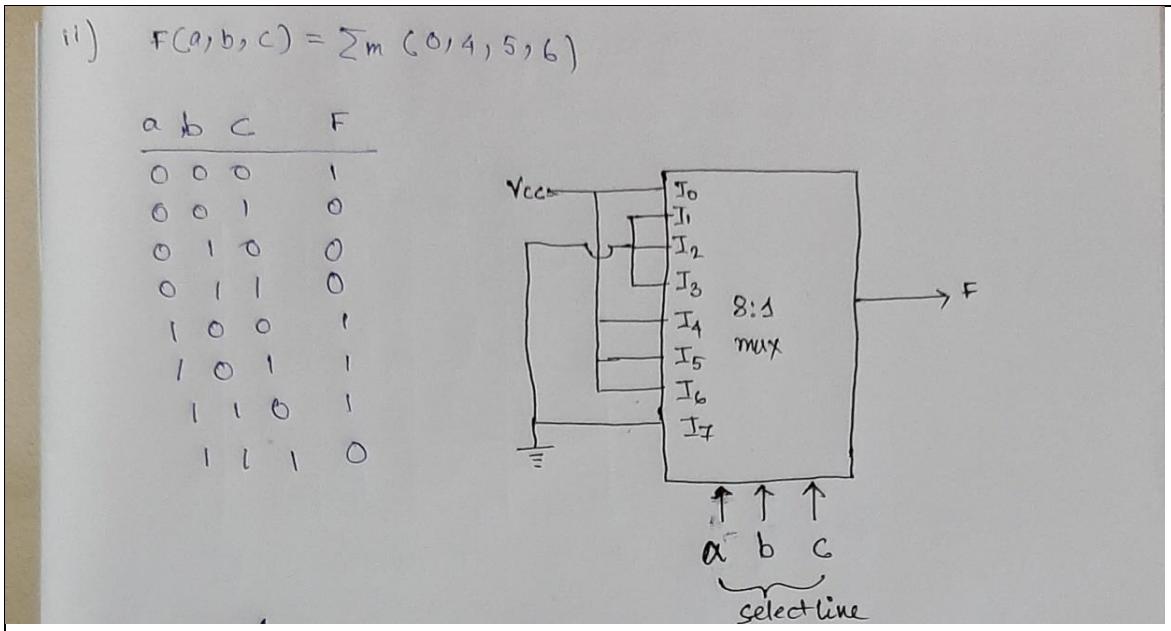
① Hazard - static-1 - hazard ie, in between 0000 → 0010

② Hazard - static-1 - hazard ie, in between 1001 → 1101

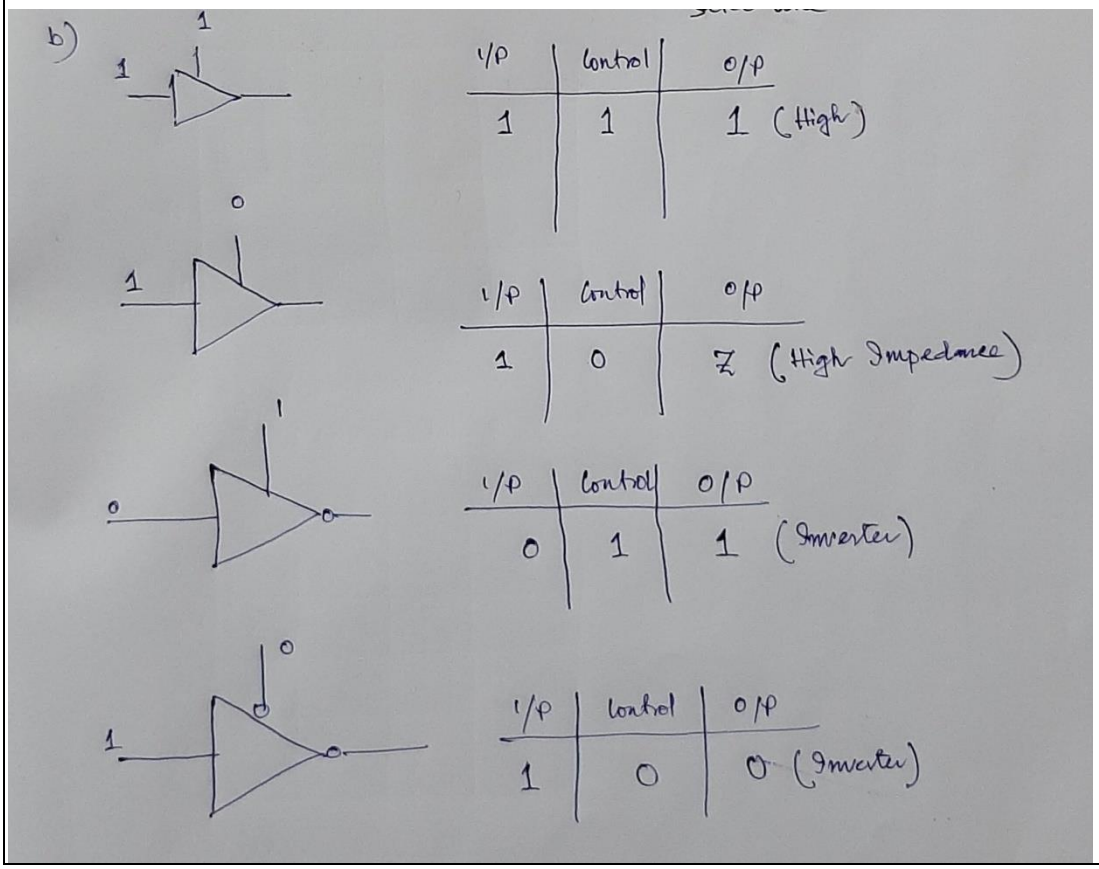
Then find an AND-OR circuit for *F* for hazards cover



7. a) i. **Explain the function of a 4 : 1 multiplexer and Implement a multiplexer using basic gates.** Answer:  **7.** **a)ii. Implement the following function using a 8 : 1 MUX F(a,b,c)=∑m(0,4,5,6) represent using Block Diagram** Answer:	[4+2]	CO4	L2,L3



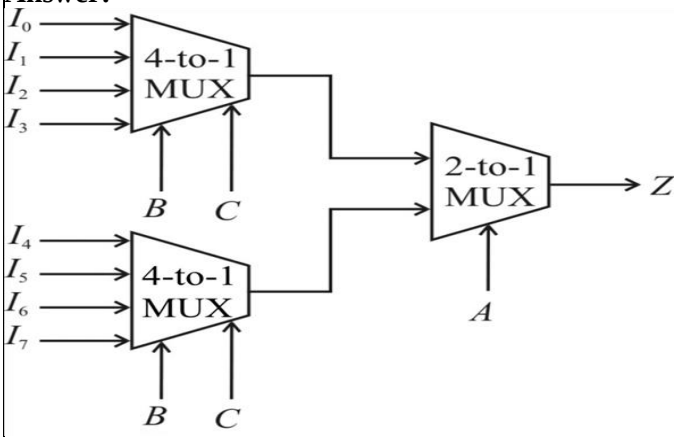
7.b) Determine the output of each three-state buffer and write truth table:	[4]	CO4	L2



8. [5+5] CO4 L3

i.Show how two 4-to-1 and one 2-to-1 multiplexers could be connected to form an 8-to-1 MUX with three control inputs.

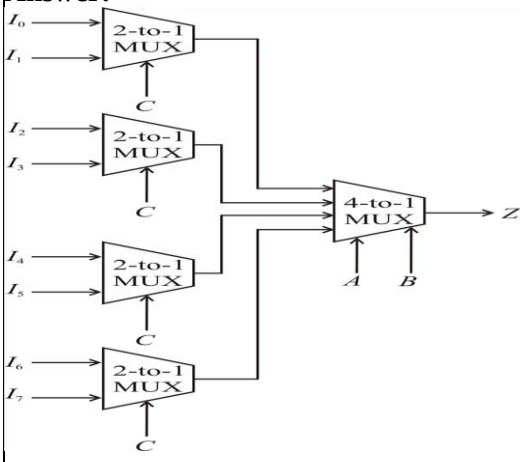
Answer: L3



Here I_0 to I_7 are inputs to multiplexer , A,B,C are selection inputs and Z is output of multiplexer

ii. Show how four 2-to-1 and one 4-to-1 multiplexers could be connected to form an 8-to-1 MUX with three control inputs.

Answer:



Here I_0 to I_7 are inputs to multiplexer , A,B,C are selection inputs and Z is output of multiplexer

9. [10] CO4 L3

Realize a full adder using a 3-to-8 line decoder

i. **two OR gates**

ii. **two NOR gates**

Answer:

Truth table full adder circuit

Input bit for number A	Input bit for number B	Carry bit input C_{IN}	Sum bit output S	Carry bit output C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table1

i.The A, B and Cin inputs are applied to 3:8 decoder as an input.

ii. The outputs of decoder m1, m2, m4 and m7 are applied to OR gate as shown in figure to obtain the sum output.

iii. Similarly outputs m3, m5, m6 and m7 are applied to another OR gate to obtain the carry output.

iv. Implement of full adder is shown in figure1.

S=∑m(1,2,4,7)-min terms

Cout=∑m(3,5,6,7)-min terms

i. Two OR gates

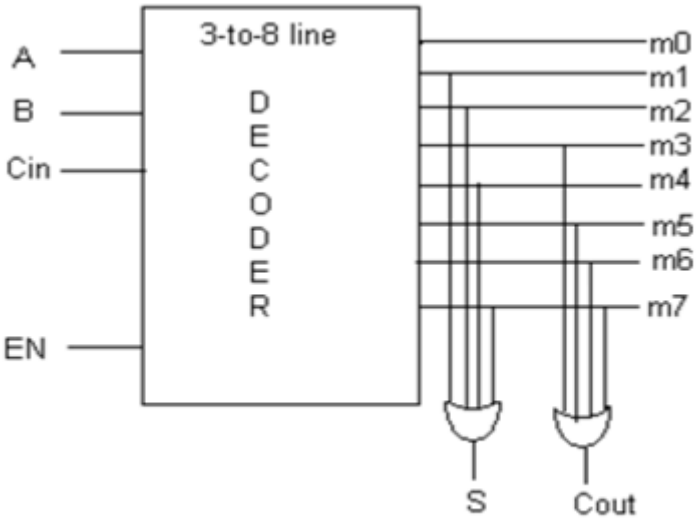


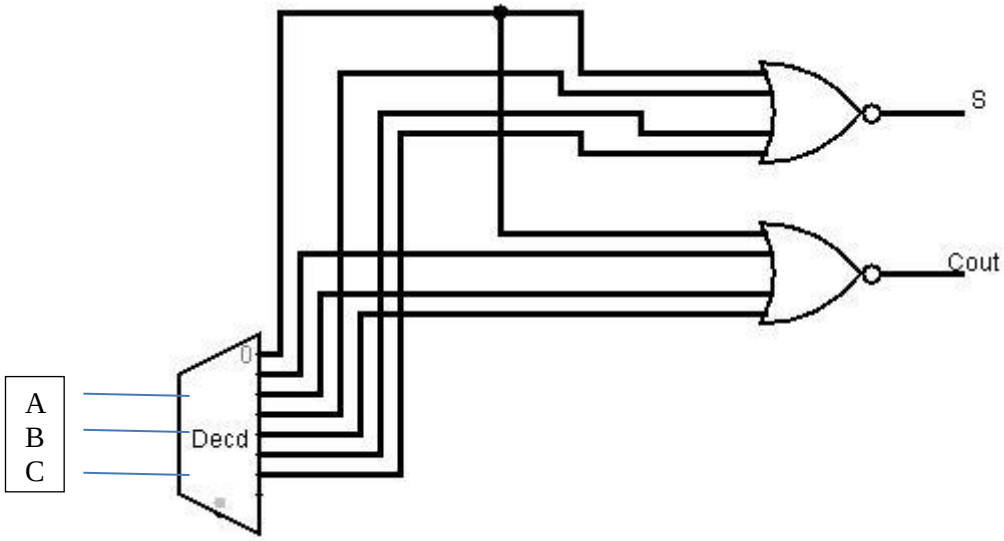
Fig1: Full Adder Implementation using 3:8 decoder

ii.TwoNOR gates

Implement of full adder is shown in figure1.

S'=∑m(0,3,5,6) –max terms

Cout=∑m(0,1,2,4)- max terms



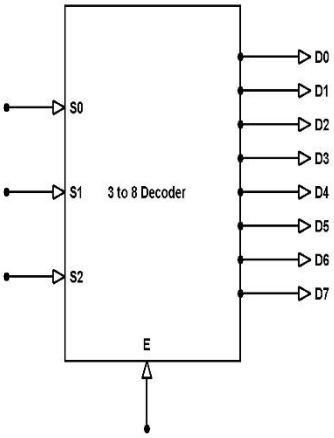
Full adder using 3 to 8 decoder

10.
i.Explain the operation of a 3 to 8 decoder and 8 to 3 encoder with Block Diagram.

[5+5] CO4 L2,L3

Answer:

3 to 8 decoder



This decoder circuit gives 8 logic outputs for 3 inputs and has a enable pin. The circuit is designed with AND and NAND logic gates. It takes 3 binary inputs and activates one of

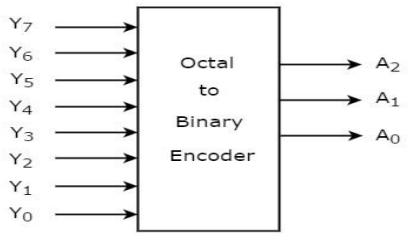
Truth table:

S0	S1	S2	E	D0	D1	D2	D3	D4	D5	D6	D7
x	X	x	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	1	0	0	1	0	0
1	1	0	1	0	1	0	0	0	0	1	0
1	1	1	1	1	0	0	0	0	0	0	1

When the Enable pin (E) is low all the output pins are low.

8 to 3 encoder: Octal to binary Encoder has eight inputs, Y_7 to Y_0 and three outputs A_2, A_1 & A_0. Octal to binary encoder is nothing but 8 to 3 encoder. The **block diagram** of octal to binary Encoder is shown in the following figure

At any time, only one of these eight inputs can be '1' in order to get the respective binary code. The **Truth table** of octal to binary encoder is shown below.



Inputs								Outputs		
Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1

0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

ii.Realize multiple output function F1(a,b,c)= ∑m(2,3,4,5) and F2(a,b,c)= =∑m(1,6,7) usingdecoder.

Answer: