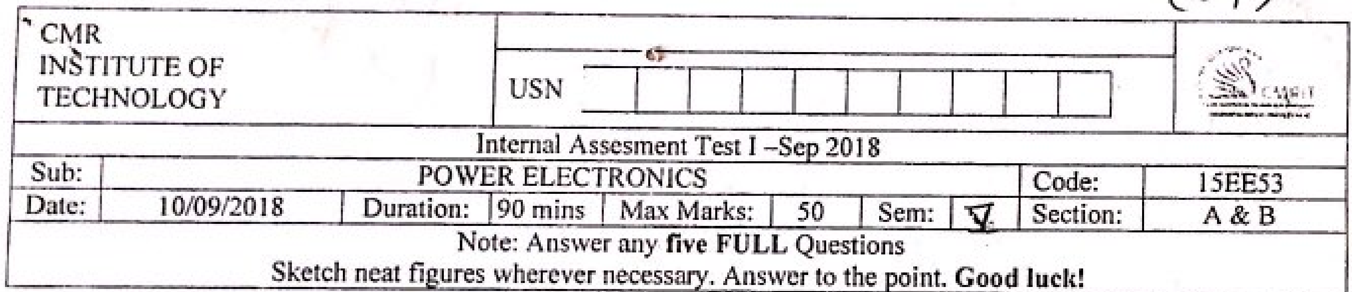
(64)



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Internal Assesment Test I –Sep 2018

Sub:	POWER ELECTRONICS							Code:	15EE53
Date:	10/09/2018	Duration:	90 mins	Max Marks:	50	Sem:	V	Section:	A & B

Note: Answer any **five FULL** Questions

Sketch neat figures wherever necessary. Answer to the point. **Good luck!**

		Marks	OBE CO	RBT
1 (a)	With neat circuit diagram ,input and output waveforms, explain the different types of power electronic circuits	[8]	CO1	L2
(b)	Discuss the major industrial applications of power electronic converter circuits	[2]	CO1	L1
2 (a)	With the help of neat waveform, explain the reverse recovery characteristics of a power diode. And also obtain an expression for peak reverse current	[10]	CO1	L2
3 (a)	With neat circuit diagram and switching times explain steady state and switching characteristics of power MOSFET	[10]	CO2	L1
4 (a)	The reverse recovery time of a diode is 5μs and rate fall of diode current is 80A/ μs Calculate i)the storage charge ii) peak reverse current	[4]	CO1	L2
(b)	The β of BJT varies from 12 to 75. The loas resistance is 1.5Ω . the supply voltage Vcc =40V and base input voltage is 6V.If V_{CEsat} = 1.2V ,V_{BEsat}= 1.6V and RB = 0.7Ω. Calculate i) ODF ii) Forced β iii) total power loss in transistor	[6]	CO2	L2

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5 (a)	List and explain the switching limits of BJT	[5]	CO2	L1
(b)	Briefly explain different types of power diodes	[5]	CO1	L1
6 (a)	Discuss the transfer and output characteristics of BJT	[5]	CO1	L1
(b)	Compare power BJT with power MOSFET	[5]	CO2	L1
7	Derive the average and rms output voltage of a single phase full bridge rectifier with R load. Also draw the related output voltage and current waveforms	[10]	CO1	L2
8	Write short notes on the following , i) Ideal characteristics of a switch ii) Practical characteristics of a switch iii) Switch specifications	[10]	CO1	L2

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TYPES OF POWER ELECTRONIC DEVICES.

The power electronic circuits are classified i[nto] six types

1. Diode rectifiers
2. AC-DC converter / controlled rectifiers
3. AC-AC converters / ac voltage controllers
4. DC-DC converters / dc choppers
5. DC-AC converters / inverters
6. Static switches.

Diode Rectifier:

→ converts ac voltage into fixed dc.

→ input could be either 1ϕ or 3ϕ.

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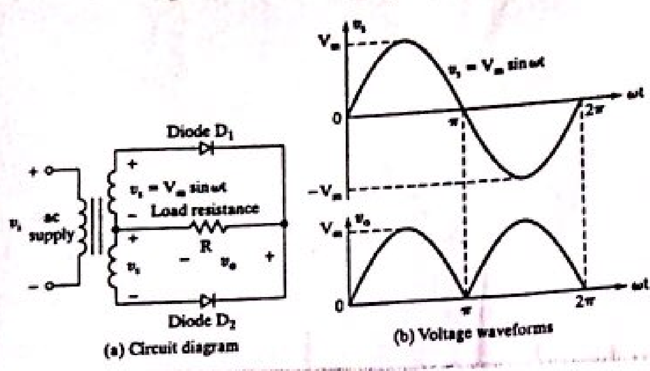
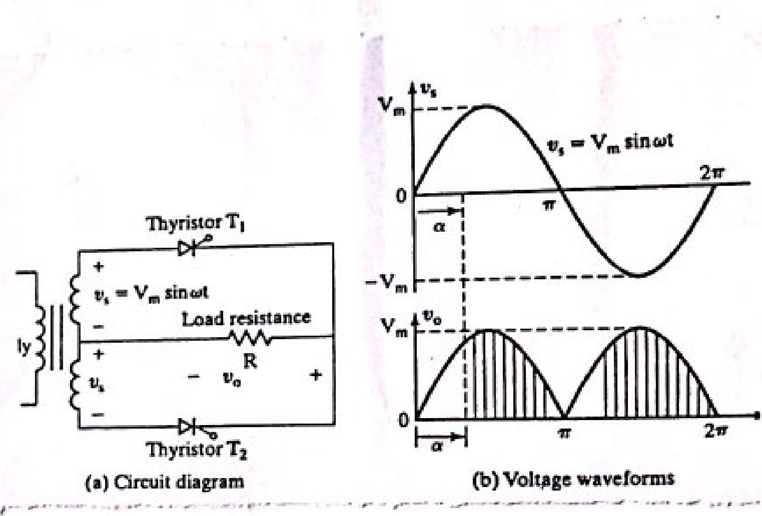


(a) Circuit diagram (b) Voltage waveforms

AC-DC Converter:- (controlled rectifiers)

The output voltage can be controlled by varying firing or triggering angle α. A single phase converter with natural commutated thyristor is shown below.

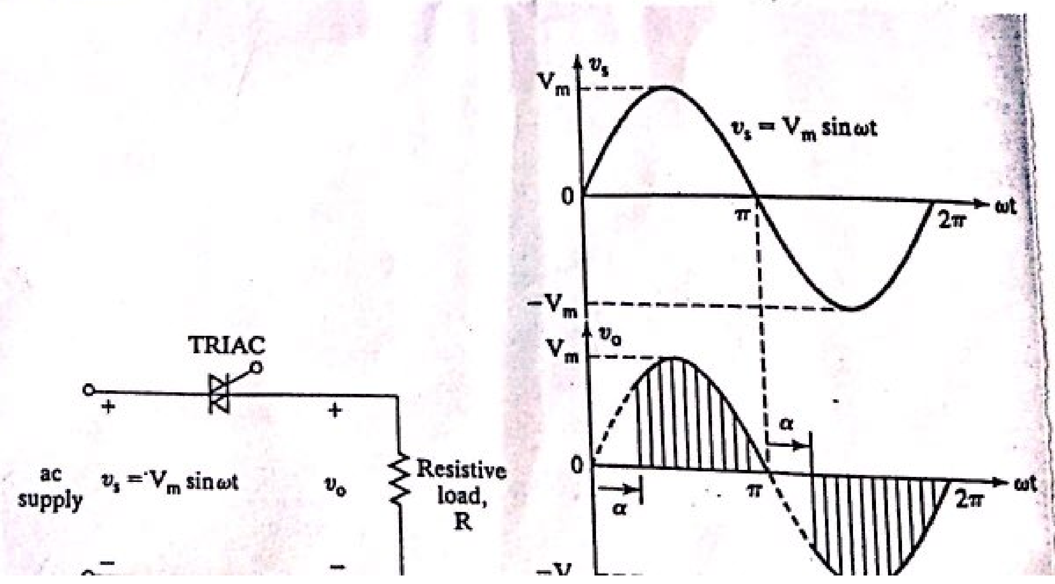


(a) Circuit diagram (b) Voltage waveforms

AC-AC Converters (ac voltage controllers)

Variable ac output voltage from fixed ac source:

A 1ϕ converter with TRIAC is shown below.



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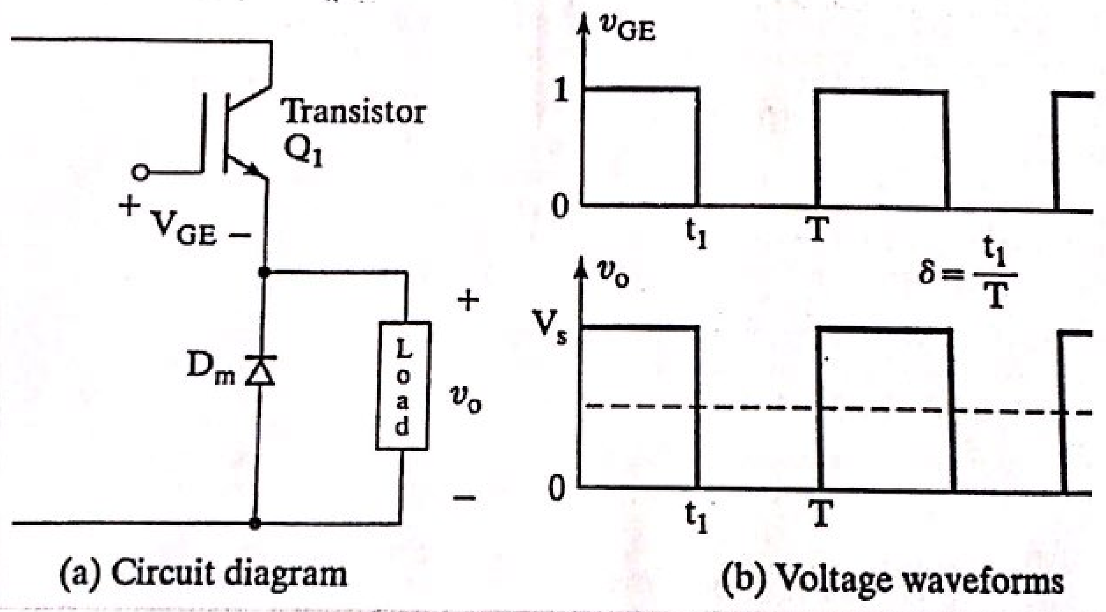
DC – DC Converters (chopper) (Switching Regulator)

To obtain variable dc voltage from fixed dc voltage. The average output voltage is controlled by varying the conduction time.

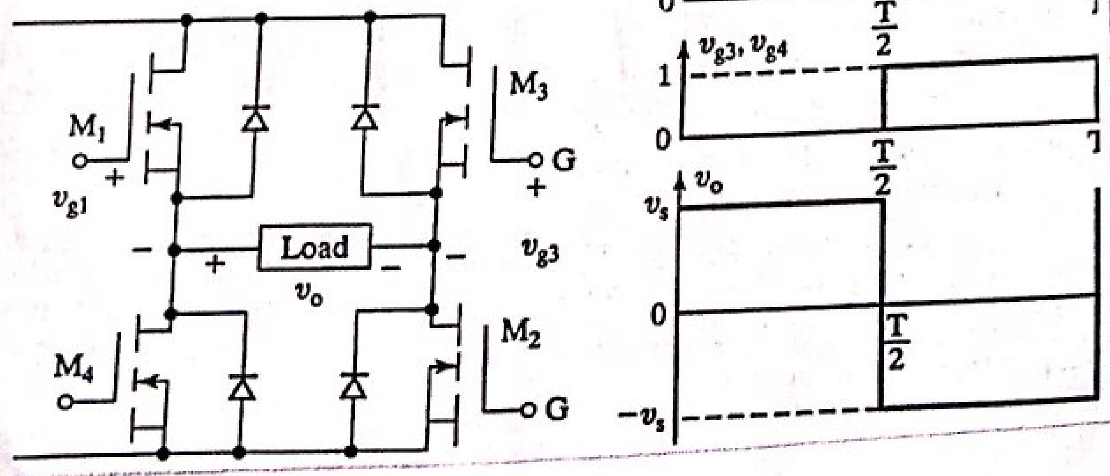


(a) Circuit diagram (b) Voltage waveforms

If T is chopping period, $t_1 = \delta T$ where δ is called duty cycle.

DC – AC Converters (inverter)

To obtain variable ac voltage from fixed dc voltage



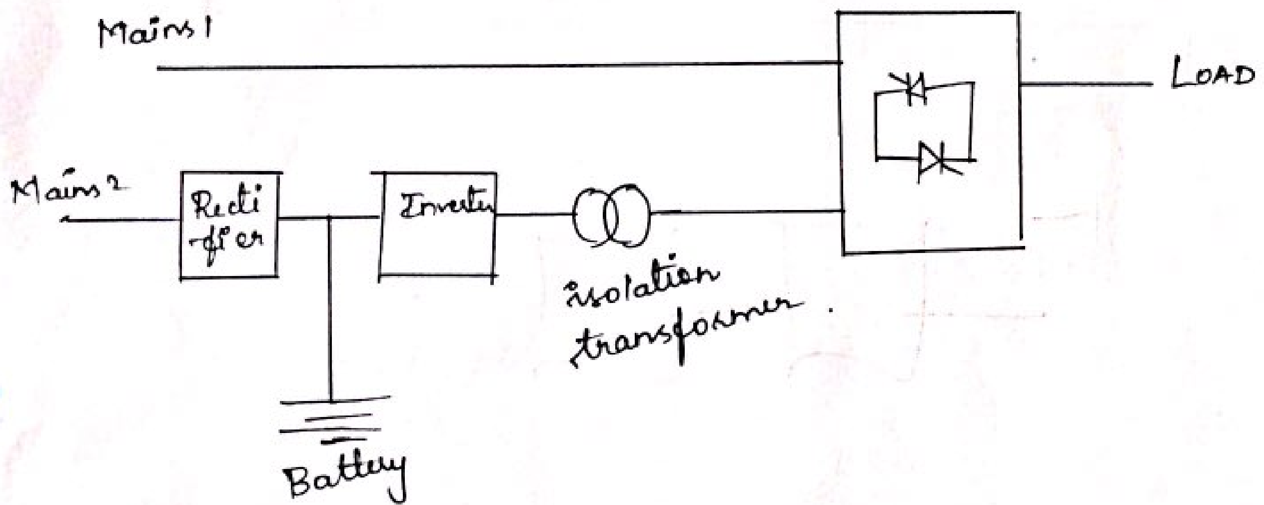
(ii)

Transistors M_1 and M_2 conduct for one half of a period and M_3 & M_4 conduct for other half. The o/p is varied by controlled the conduction time of the transistors.

Static Switches :- (ac or dc static switches)

Power electronic devices used as static switches in an UPS is shown below.

Mains1 and mains2 are connected to same supply.



Power electronics - now used in a great variety of high - power products,

* heat controls
* light controls
* motor controls
* power supplies
* vehicle propulsion systems
* HVDC systems
* FACTs.

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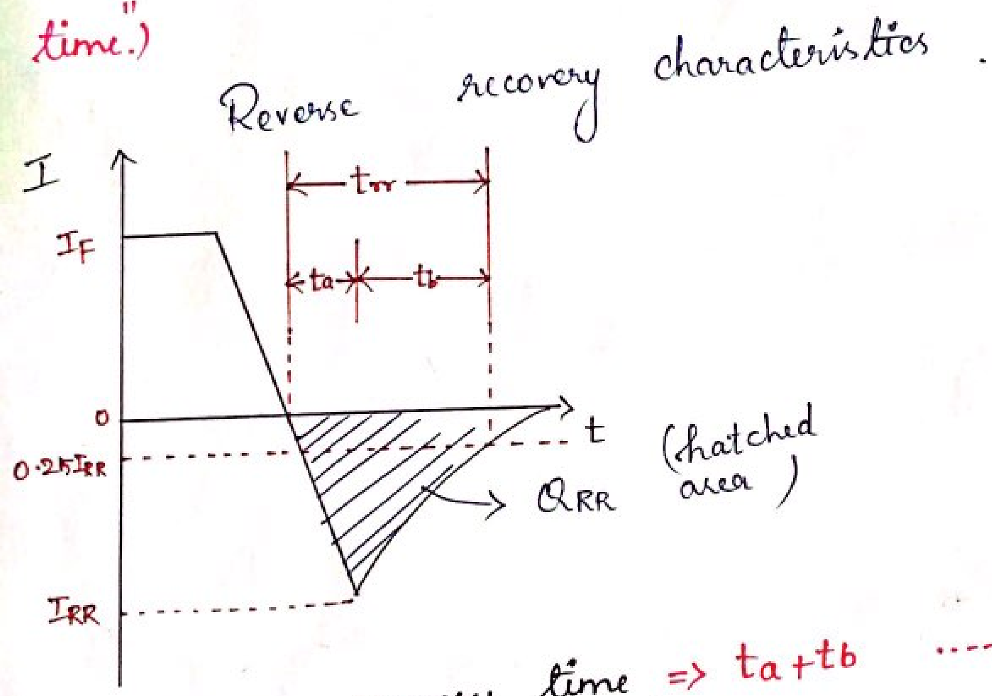
Reverse Recovery Characteristics:

→ The current in diode is due to net effect of majority and minority carriers

Once the diode current is reduced to zero (application of reverse voltage), the diode continues to conduct due to minority carriers in junction and semi-conductor material. This carriers require certain time to recombine and neutralize called "reverse recovery time.")

Reverse recovery characteristics.



t_{rr} - reverse recovery time => $t_a + t_b$ ..... (1)

- measured from initial zero crossing of diode current to 25% of max reverse current I_{RR}

t_a - due to charge stored in the depletion region of jxn.

- time b/w zero crossing and I_{RR}

t_b - due to charge stored in the material

$\frac{t_b}{t_a}$ => softness factor (S)

if $S \geq 1$ → soft recovery.

$S < 1$ → fast recovery.

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The peak reverse current is given by,

$$I_{RR} = t_a \frac{di}{dt} \quad \ldots\ldots \quad (2)$$

Reverse recovery charge Q_{RR} – the amt of charge carriers that flows across the diode in reverse dir due to changeover from forward conduction to reverse blocking condition.

$$Q_{RR} \cong \frac{1}{2} I_{RR} t_a + \frac{1}{2} I_{RR} t_b$$

(area – considering triangle $= \frac{1}{2} \times l \times b$)

$$= \frac{1}{2} I_{RR} t_{rr}$$

$$I_{RR} \cong \frac{2Q_{RR}}{t_{rr}} \quad \ldots\ldots \quad (3)$$

using (2) and (3),

$$t_a \frac{di}{dt} = \frac{2Q_{RR}}{t_{rr}}$$

assume $t_b << t_a$, i.e $t_{rr} \approx t_a$

$$t_{rr} t_a = \frac{2Q_{RR}}{di/dt}$$

$$t_{rr}^2 = \frac{2Q_{RR}}{di/dt}$$

$$t_{rr} = \sqrt{\frac{2Q_{RR}}{di/dt}} \quad \ldots\ldots \quad (4)$$

~~using (3) and (4),~~

~~$$I_{RR} = \frac{2Q_{RR}}{t_{rr}} \sqrt{\frac{2Q_{RR}}{di/dt}}$$~~

~~$=$~~

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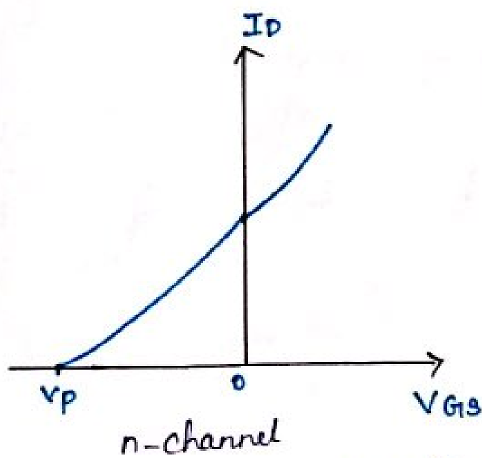
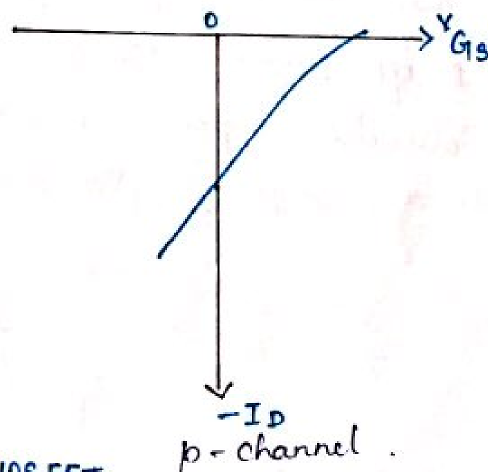
Steady state characteristics :-

- Mosfets are voltage controlled devices with very high input impedance and gate draws a very small leakage current in the order of nano-amperes.
- very high current gain $\frac{I_D \ (o/p)}{I_G \ (i/p)} \cong 10^9$
- However in case of MOSFETS, rather than current gain, there is an another important parameter called transconductance

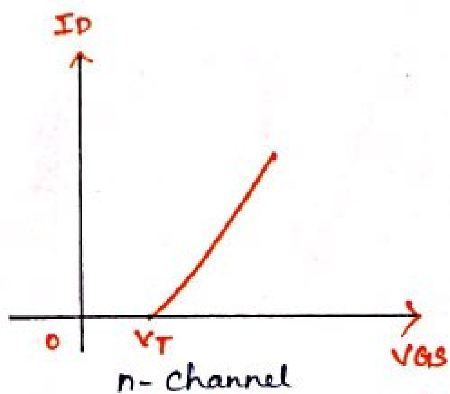
$$\text{transconductance} = \frac{I_D}{V_{GS}} \left[\frac{\text{drain current}}{\text{gate voltage}} \right]$$

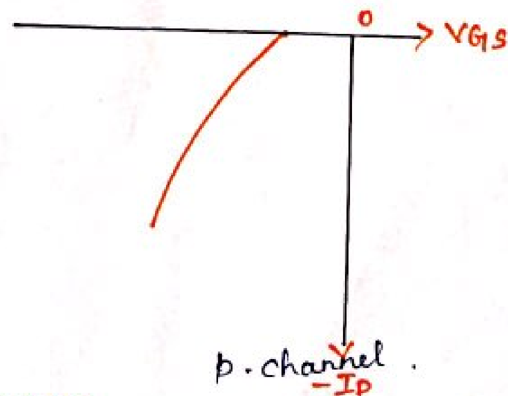
The transfer characteristics of n-channel and p-channel MOSFETS are shown below.





(i) depletion type MOSFET





(ii) Enhancement type MOSFET

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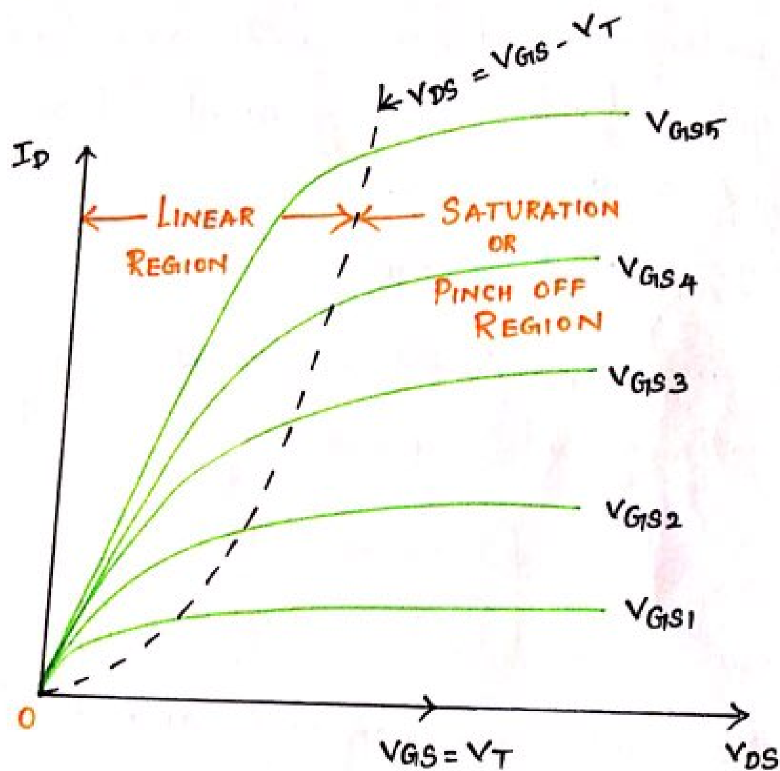
Output Characteristics :- (n-channel enhancement MOSFET)



$V_{GS5} > V_{GS4} > V_{GS3} > V_{GS2} > V_{GS1} > V_T$

the o/p characteristics $I_D - V_{DS}$ is shown above.

There are three region of operation

1. cut off region $V_{GS} \leq V_T$
2. Saturation region $V_{DS} \geq V_{GS} - V_T$
3. Linear region $V_{DS} \leq V_{GS} - V_T$.

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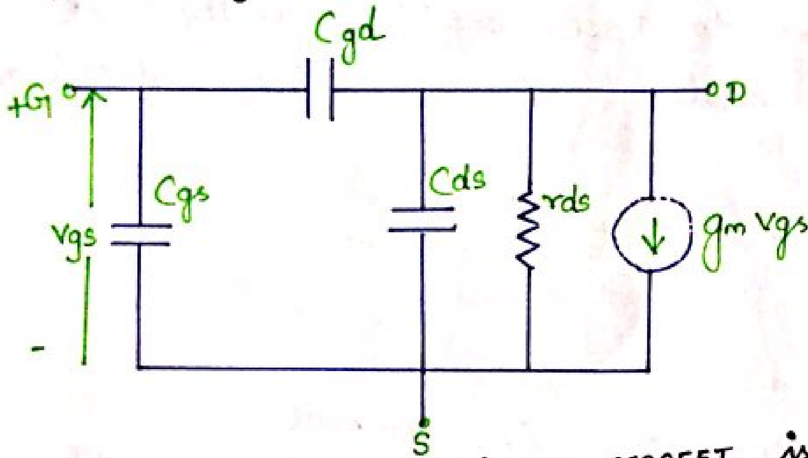
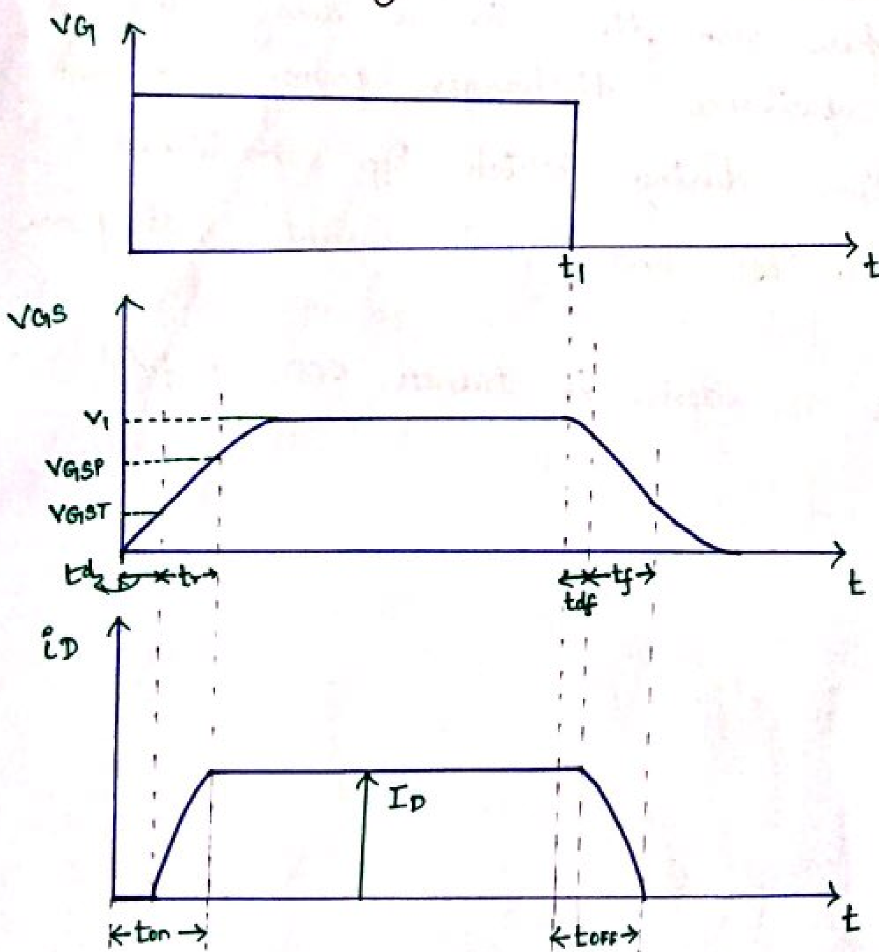
SWITCHING CHARACTERISTICS :-

* The switching characteristics of MOSFET are influenced by internal capacitance of the device and internal impedance of the gate driver circuit.



* The switching model of MOSFET is shown in figure



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↳ When +ve gate voltage is applied, the device doesn't turn ON instantly, it requires some time delay for the input capacitance to charge to gate threshold voltage V_{GST}.

↳ This time delay is called as turn-on time delay (t_{dn})

↳ There is a further delay called rise time t_r during which gate voltage rises to V_{GSP} (sufficient voltage to drive MOSFET into on state) and I_D rises from zero to full-on current.

turn-on time = delay time + rise time

$$t_{on} = t_{dn} + t_r$$

↳ At time t_1, when gate-voltage is removed, the turn OFF process is initiated (since MOSFET is majority carrier device) and here also there is a delay time during which input capacitance discharges from V_1 to V_{GSP}

↳ Fall time t_f - the time during which i/p capacitance discharges from V_{GSP} to V_{GST} and drain current falls from I_D to zero.

↳ When $V_{GS} \leq V_{GST}$ - the device is turned OFF completely.

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using (3) and (4),

extra

CMR

② If the reverse recovery time of a diode is $5\mu s$ and the rate of decay of the diode current is $50A/\mu s$ calculate i) Q_{RR} ii) I_{RR}.

Given $t_{rr} = 5\mu s$, $\frac{di}{dt} = 50A/\mu s$

$= 5\times10^{-6}s$ $\quad\quad = 50\times10^{6}\ A/s$

$$Q_{RR} = \frac{1}{2}\frac{di}{dt}t_{rr}^2$$

$$= \frac{1}{2}\frac{di}{dt}\times t_{rr}^2 \Rightarrow \frac{1}{2}\times50\times10^{6}\times(5\times10^{-6})^2$$

$$\boxed{Q_{RR} = 625\mu C}$$

$$I_{RR} = \sqrt{2Q_{RR}\frac{di}{dt}}$$

$$= \sqrt{2\times625\times10^{-6}\times50\times10^{6}}$$

$$\boxed{I_{RR} = 250A}$$

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② $\beta \to 12$ to 75, $R_C = 1.5\Omega$, $V_{CC} = 40V$, $V_B = 6V$,

$V_{CE}(sat) = 1.2V$, $V_{BE}(sat) = 1.6V$ and $R_B = 0.7\Omega$. find)

i) ODF (ii) β_{forced} (iii) P_T.

$$ODF = \frac{I_B}{I_{BS}} \; ; \quad I_B = \frac{V_B - V_{BE}(sat)}{R_B} \Rightarrow \frac{6 - 1.6}{0.7} \Rightarrow 6.29A.$$

$$I_{BS} = \frac{I_{CS}}{\beta} \; ; \quad I_{CS} = \frac{V_{CC} - V_{CE}(sat)}{R_C} \Rightarrow \frac{40 - 1.2}{1.5} \Rightarrow 25.87A.$$

$$I_{BS} = \frac{25.87}{\beta_{min}} \Rightarrow \frac{25.87}{12} \Rightarrow 2.15A.$$

$$ODF = \frac{6.29}{2.15} \Rightarrow 2.91 \approx 3$$

$$\boxed{ODF = 3}$$

ii) $$\beta_{forced} = \frac{I_{CS}}{I_B} \Rightarrow \frac{25.87}{6.29} \Rightarrow 4.1128$$

iii) $$P_T = V_{BE} I_B + V_{CE} I_C$$

$$= (1.6 \times 6.29) + (1.2 \times 25.87)$$

$$P_T = 41.108.$$

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SWITCHING LIMITS

↳ Secondary breakdown
↳ Safe operating area SOA
↳ Power derating
↳ Breakdown voltages.

Secondary breakdown:

* failure mode in BJTs. In a power transistor with large junction area, under certain cond of current and voltage, the current concentrates in small spots of BEJ.
* This causes localised heating, progressing into a short b/w collector and emitter which can destroy the transistor.

Safe Operating Area:-

↳ forward - biased SOA
↳ reverse - biased SOA

→ the safe operating limits of collecting current I_C versus collector - emitter voltage V_{CE}. - for reliable operation of the transistor, the collector current and voltage must always lie within this area.

Forward biased SOA:- (FBSOA)

during on-state conds, the avg jxn temp and secondary breakdown limit the power handling capability of transistor. The manufacture always provide FBSOA curve which indicates the I_C - V_{CE} limits under forward biased conditions.

Reverse biased SOA :- RBSOA

during turn-off, a high current and high voltage must be sustained by the transistor with BJT reverse biased. The manufacture provides the $I_C - V_{CE}$ limits during reverse-biased turn-off as RBSOA.

Power derating :-

The power derating factor of a transistor is the amount by which the power dissipating rating of a transistor falls when the transistor junction temperature increases.

The power dissipation rating of a transistor is usually given at 25°C.

Manufacturers usually supply the derating factors for determining power dissipation at any temperature above 25°C. The derating factor is specified in W/°C.

Eg:- 2mW/°C - for each 1° rise in temperature of the transistor is reduced by the power rating 2mW.

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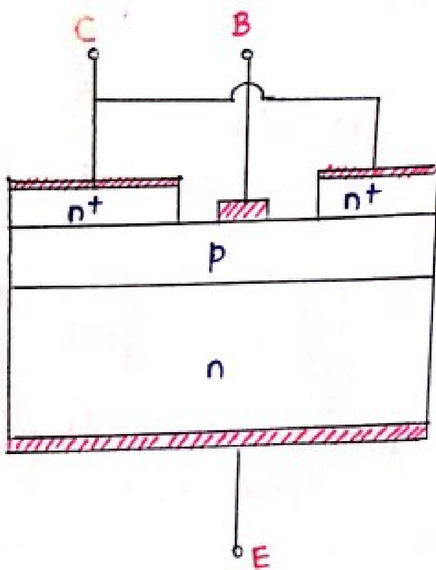
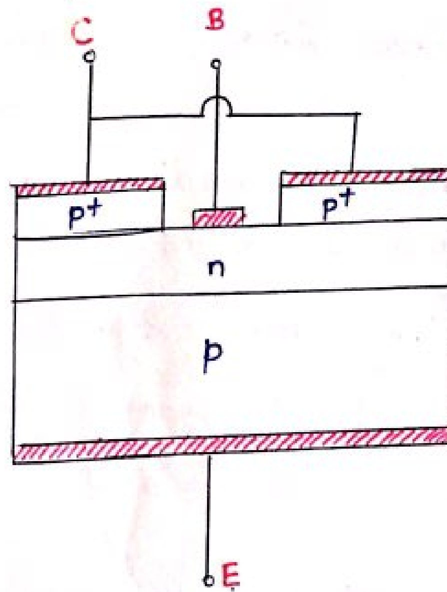
Cross sectional view of BJT





NPN

↳ E side n-layer - wider
p-layer - narrow

↳ C side n-layer - narrow and heavily doped.

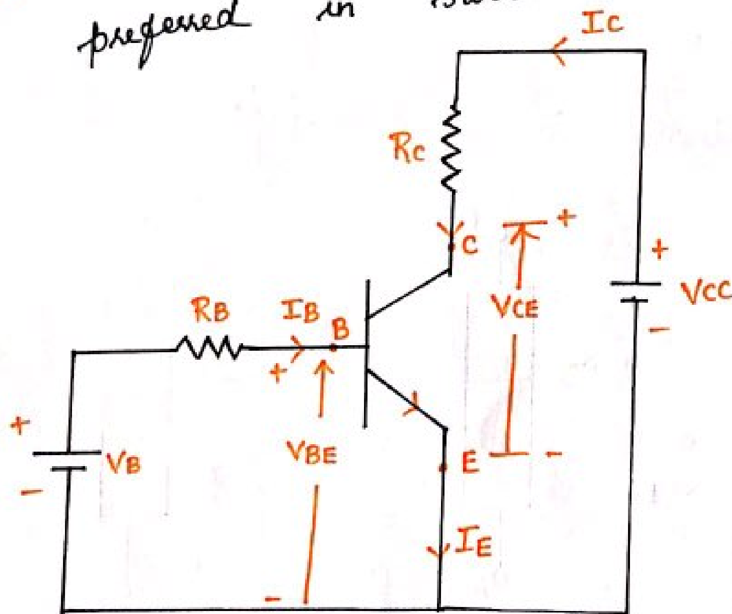
PNP

↳ E side p-layer - wider
n-layer - narrow

↳ C side p-layer → narrow and heavily doped.

Steady - state characteristics :-

Common - emitter configuration is taken which is generally prefered in switched application.



Input Characteristics: (I_B Vs V_{BE} keeping const V_{CE})

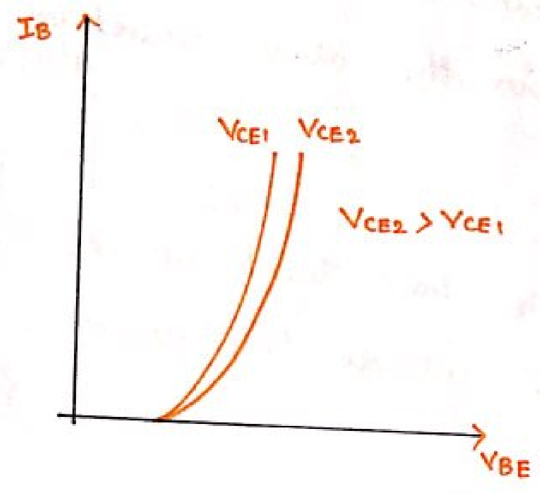


FIG 1

Output Characteristics: (I_C Vs V_{CE})

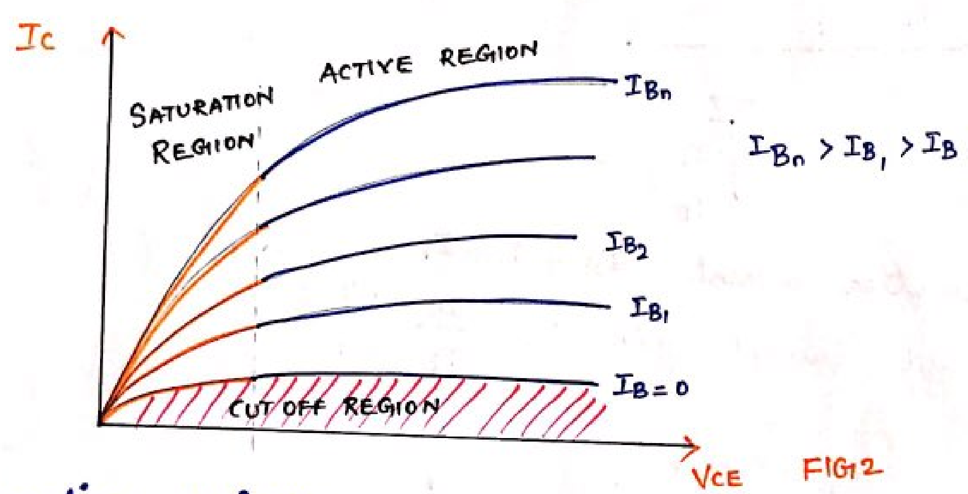


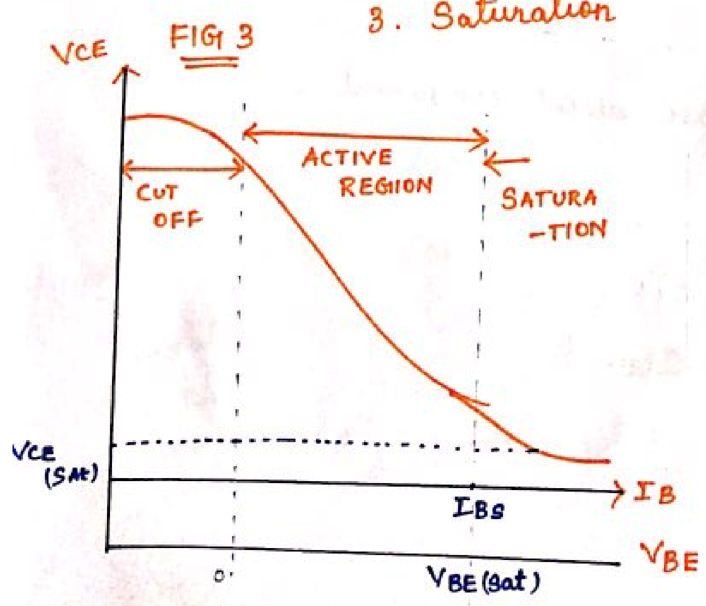
FIG 2

$I_{B_n} > I_{B_1} > I_B$

Three - operating regions:

1. cut-off
2. Active
3. Saturation

FIG 3



* CUT-OFF REGION:-

→ Transistor is OFF - I_B is not sufficient to turn on it

→ Both the jxns CBJ and BEJ are reverse biased

* ACTIVE REGION:-

→ Transistor acts as an amplifier

→ V_{CE} ↓s with ↑s in I_B

→ CBJ is RB and BEJ is FB

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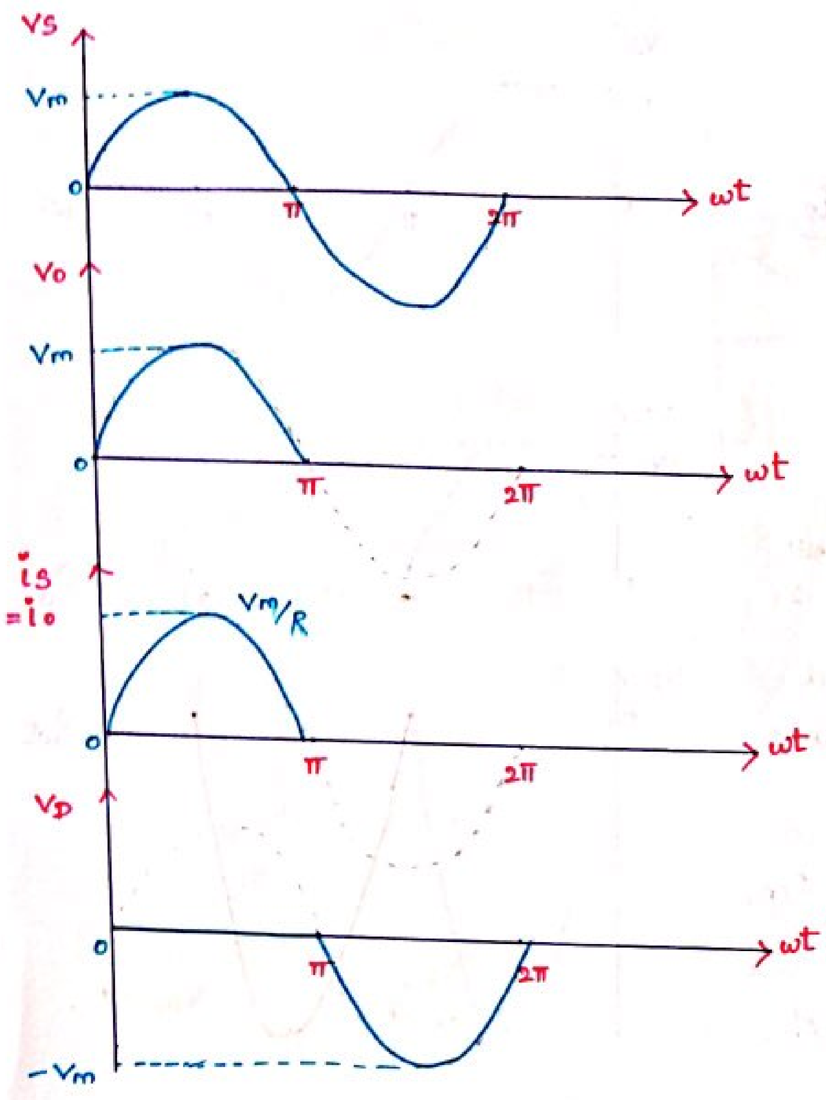
COMPARISION OF BJT - MOSFET

MOSFET	BJT
1. Unipolar device	1 Bipolar device
2. High input impedance (mega ohm)	2. Comparitively low input impedance. (KΩ)
3. Low switching losses but high conduction losses	3. High switching losses and low conduction loss.
4. High frequency applications	4. Low frequency applications
5. Voltage controlled device	5. current controlled device.
6. +ve temp - co eff for resistance - easy parallel operations	6. -ve temp co-eff - current sharing resistors necessary for parallel operations
7. Secondary breakdown doesnot occur.	7. Secondary breakdown occurs.
8. Limited voltage rating bcoz of more conduction loss - 500V, 140A rating	8. BJTs with rating 1200V, 800A are available.



FULL WAVE RECTIFIERS

There are two types of single phase full-wave rectifiers,

- Center-tapped transformer
- Bridge type

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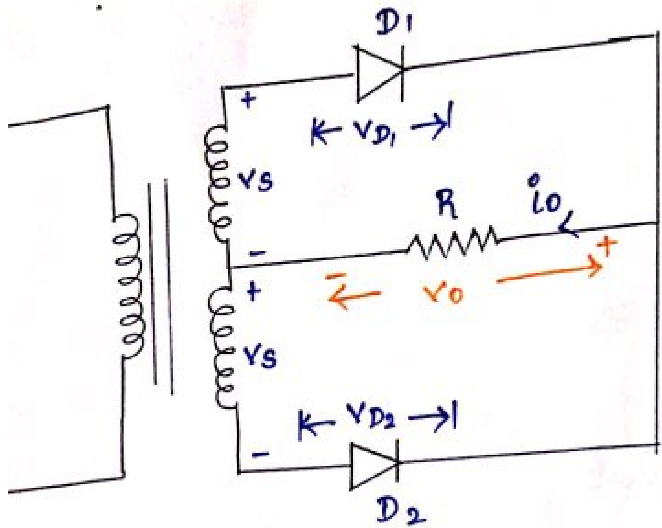
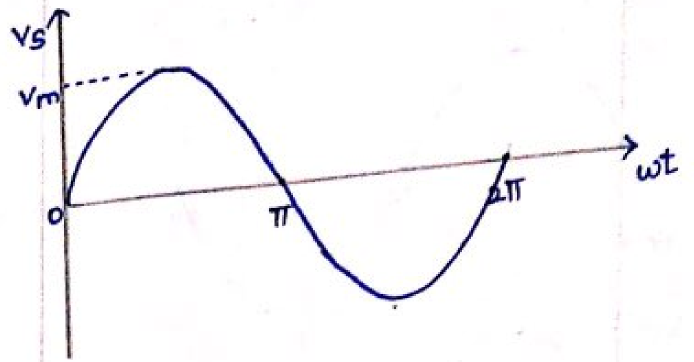
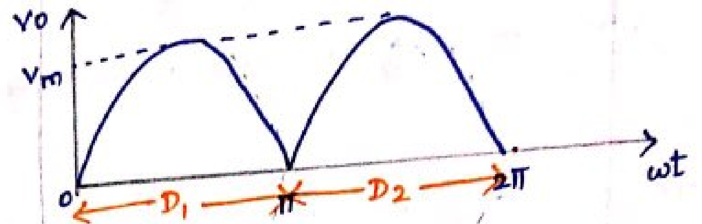
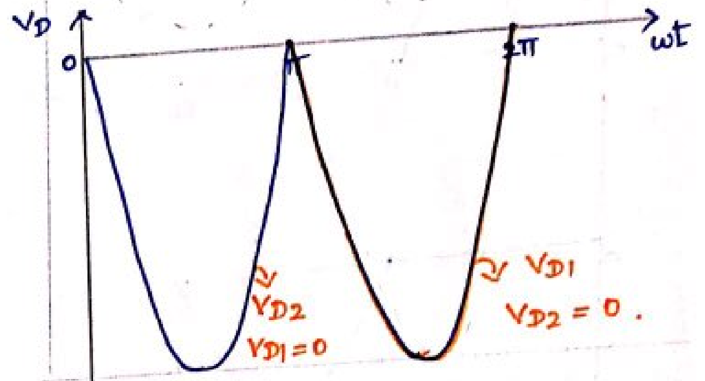
he waveform for current









CENTER TAPPED TRANSFORMER

During first half cycle D_1 gets forward biased and source voltage appears across the load

During -ve half cycle of i/p, D_2 gets forward biased and load gets connected to the source.

The source, output voltage and the voltage across diode is shown in the above waveforms.

The average o/p voltage is,

$$V_{dc} = \frac{1}{\pi} \int_0^{\pi} V_m \sin \omega t \, d\omega t$$

$$= \frac{V_m}{\pi} \int_0^{\pi} \sin \omega t \, d\omega t$$

$$= \frac{V_m}{\pi} \left(-\cos \omega t \right)_0^{\pi}$$

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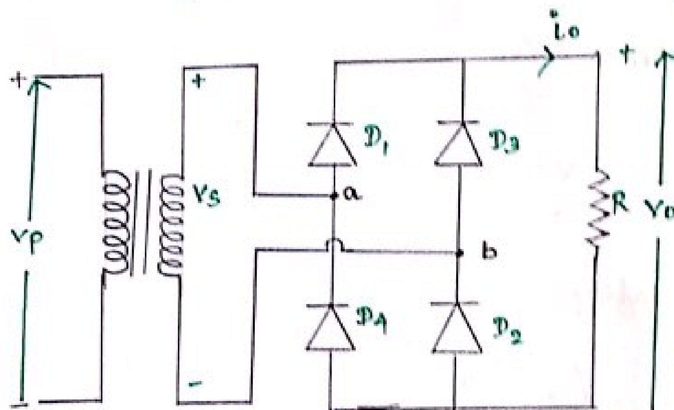
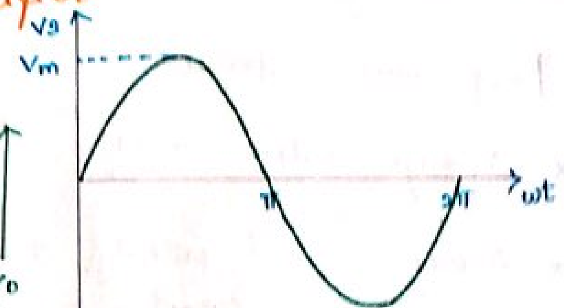
$$= \frac{V_m}{\pi}[-\cos\pi + \cos 0]$$

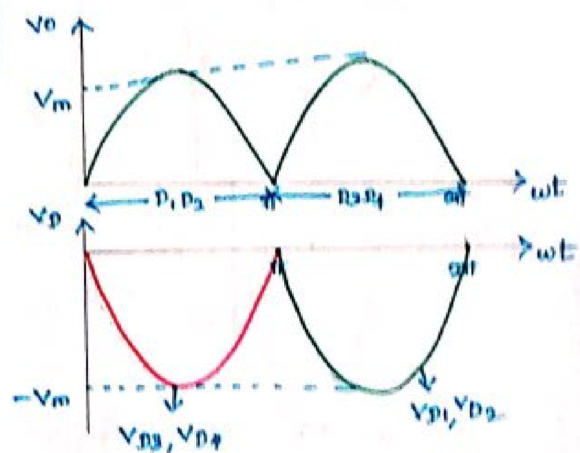
$$= \frac{V_m}{\pi}[-(-1)+1]$$

$$V_{dc} = \frac{2V_m}{\pi} \quad (\text{or}) \quad 0.6366V_m$$

Instead of using center-tapped transformer, full-wave rectifier can be obtained using four diodes called full-wave bridge rectifier







* During +ve half cycle, D_1D_2 gets forward biased, load gets connected to the source and the current flows from (a) $V_s - D_1 - R, - D_2 - V_s$ (b)

* During −ve half cycle, D_3D_4 gets forward biased and current flows from (b) $V_s - D_3 - R - D_4 - V_s$ (a).

The corresponding voltage and current waveform are shown in the figure.

The ...

D_1 V_s

⇒ It should be noticed that in case of center-tapped transformer, the peak inverse voltage (PIV) is $2V_m$, whereas in case of bridge rectifier PIV is only V_m.

⇒ center-tapped transformer configuration requires only two diodes whereas bridge rectifier requires four diodes.

Performance parameters :-

* Average output voltage, $V_{dc} = \frac{2V_m}{\pi}$

* Average load / output current, $I_{dc} = \frac{V_{dc}}{R} \Rightarrow \frac{2V_m}{\pi R}$.

* RMS value of the output voltage,

$$V_{rms} = \left[\frac{1}{\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t \; d\omega t\right]^{1/2}$$

$$V_{rms}^2 = \frac{1}{\pi} V_m^2 \left[\int_0^{\pi} \left(\frac{1-\cos 2\omega t}{2}\right) d\omega t\right]$$

$$= \frac{V_m^2}{2\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_0^{\pi}$$

$$= \frac{V_m^2}{2\pi}\left[(\pi - 0) - \frac{\sin 2\pi + \sin 0}{2}\right]$$

$$= \frac{V_m^2}{2}$$

— WITH RL LOAD:-

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$\boxed{V_{rms} = 0.707 V_m}$$

$$I_{rms} = \frac{V_{rms}}{R}$$

$$\boxed{I_{rms} = \frac{0.707 V_m}{R}}$$

O/p ac power = $V_{rms} I_{rms}$

$$= \frac{0.707 V_m \times 0.707 V_m}{R}$$

$$= \frac{0.4998 V_m^2}{R}$$

o/p dc power = $V_{dc} I_{dc}$

$$= \frac{2V_m}{\pi} \times \frac{2V_m}{\pi \times R}$$

$$= \frac{0.4053 V_m^2}{R}$$

Rectification ratio or efficiency $\eta = \frac{P_{dc}}{P_{ac}}$

$$= \frac{0.4053 V_m^2}{R} \times \frac{R}{0.4998 V_m^2}$$

$$\boxed{\eta = 81.09\%}$$

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. I_{leak} increases during turn ON and OFF time.

Characteristics and specification of switches

* Ideal characteristics
* Practical characteristics
* Switch specifications
* Device choices.

Ideal Characteristics:

1. Switch - ON state → i) ability to carry high forward current I_F (∞), ii) V_{ON} (0) - low on state forward voltage drop iii) R_{ON} (0) – low on-state resistance - ∴ power loss P_{ON} is also zero.
2. Switch OFF state → i) VBR - ability to withstand high voltage ∞ – reverse voltage ii) I_{OFF} - low off-state leakage current (zero) iii) high off - state resistance R_{OFF} (∞) – P_{OFF} (zero).
3. The TURN ON – TURN OFF process should be instantaneous → i.e LOW delay time t_d, rise time t_r, storage time t_s, fall time t_f (all tending to zero). and also it must require low gate-driver power P_G, gate-drive voltage V_G, gate drive current I_G → all tending to zero.

→ the ON- OFF process should be controllable (gate signal).

4. the switch should be capable of handling rapid changes in voltage and current i.e high $\frac{dv}{dt}$ and $\frac{di}{dt}$ rating and it should also have high i^2t
5. Negative temp co-efficient – to result in equal current rating – when operated in parallel.

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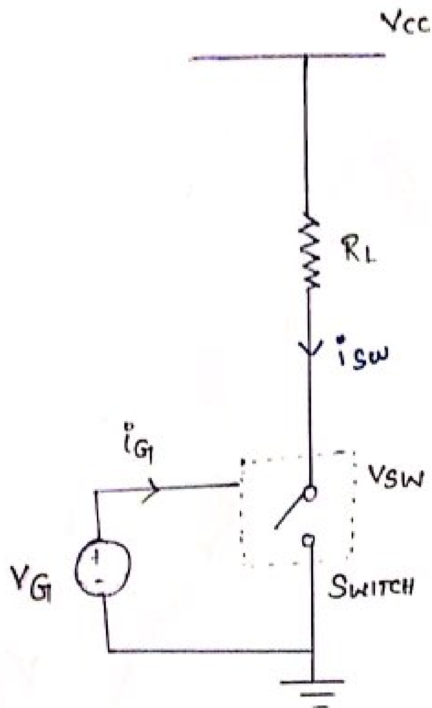
... increases during turn ON and OFF time.

PRACTICAL CHARACTERISTICS:



→ A practical switch will have FINITE t_d, t_r, t_s, and t_f.

Turn on time $= t_d + t_r \Rightarrow t_{ON}$

Turn off time $= t_s + t_f \Rightarrow t_{OFF}$

→ The waveforms for device voltage and current are shown in figure.

→ The practical switch dissipates some energy during conduction and switching.

P_{ON} - the average conduction power loss

$$= \frac{1}{T_S} \int_0^{t_{ON}} p \, dt$$

where T_S - conduction period

p - instantenous power $\Rightarrow V_{sw} \times i_{sw}$

V_{sw} - voltage drop across switch

i_{sw} - conducted current.

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* power losses increases during turn ON and OFF time.

∴ power dissipation of a switching device

$$P_D = P_{ON} + P_{SW} + P_G$$

P_{ON} - average conduction power loss

P_{SW} - switching power loss

$$= f_s \left[\int_0^{t_r} p\,dt + \int_0^{t_s} p\,dt + \int_0^{t_f} p\,dt \right]$$

↳ switching fre ($1/T_s$)

P_G - gate drive power.

SWITCH SPECIFICATIONS :- (DATA SHEET)

* voltage ratings
* Current ratings
* Frequency or switching speed
* di/dt rating
* dv/dt rating
* Switching losses
* Gate drive requirements
* SOA - safe operating area
* I^2t for fusing
* Temperature
* Thermal resistance.

DEVICE CHOICES :-

* High power applications → thyristors
* Low " " → initially MOSFETs, BJTs - now-a-days slowly replaced by COOLMOSs & IGBTs

* High power applications with forced commutation - GTOs and IGCTs.