## 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice. Important Note: 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

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## Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020 **Embedded Computing Systems**

Max. Marks: 100

Note: Answer any FIVE full questions, selecting at least TWO questions from each part.

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		IARTA	
1	a.	What is an embedded system? Explain the characteristics of embedded system.	(05 Marks)
	b.	Mention the major steps in the embedded system design process. With neat	diagrams,
		explain the various design process in the GPS moving map.	(10 Marks)
	c.	Explain the state diagram for panel-active behavior in modern train controller.	(05 Marks)
2	a.	Differentiate the following with an example: (i) Von-Neuman and Hardward a	rchitecture
_		(ii) Segmentation and paging	(06 Marks)
	b.	Draw a UML sequence diagram and write a program for copying characters from	an input to
		an output device using interrupt-driven I/O. The diagram should include two I/O	O handlers
		and the foreground program.	(08 Marks)
	c.	Mention the limitations of direct-mapped cache. How to overcome the limitations	Explain.
			(06 Marks)
3	a.	Discuss the requirement chart of a Alarm clock.	(08 Marks)
	b.	Explain the different types of debugging techniques.	(08 Marks)
	c.	With a neat sketch, explain the glue logic interface.	(04 Marks)
4	a.	Consider the following 'C' code statement $a * b + 5 * (c - d)$ .	
		i) Draw the DFG for the above 'C' statement.	
		ii) Generate the ARM assembly code for the above 'C' statement.	(06 Marks)
	b.	Explain the circular buffers for the embedded programs.	(04 Marks)
	c.	Explain the different types of program, optimization techniques.	(10 Marks)
		$\underline{PART - B}$	
5	a.	With a neat sketch, explain the operating system architecture.	(10 Marks)
	b.	Three processes with process IDs P1, P2, P3 with estimated completion tim	e 10, 5, 7
		milliseconds respectively enters the ready queue together in the order P1, P2, P3	3. Calculate
		the waiting time and Turn Around Time (TAT) for each process and the average	ige waiting
		time and TAT. (Assuming there is no I/O waiting for the processes).	(08 Marks)
	c.	What is the significance of spin lock?	(02 Marks)
=	To be designed in		(00.34   1.3
6	a.	Explain different types of interprocess communication with an example.	(08 Marks)
	b.	What are the factors need to be evaluated in selection of an RTOS? Explain.	(06 Marks)
	c.	Explain the system architecture of an answering machine.	(06 Marks)
-	_	Final-in the terminal has transportions on the I <sup>2</sup> C has with a timing diagram	(05 Marks)

Explain the typical bus transactions on the I<sup>2</sup>C bus with a timing diagram. (05 Marks) (05 Marks)

Explain the structure of IP packet. b.

Discuss the basic class diagram for the elevator system. Include \* classes for the physical interfaces (user interface) of the elevator control panels, floor control panels and displays. (10 Marks)

Explain the different types of files generated during cross compilation. (10 Marks) 8

Explain the following: (i) Incremental EEPROM Burning Technique

(ii) In circuit Emulator (Z<sub>CE</sub>) Based Firmware Debugging. (10 Marks)

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