USN

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020
Advanced Computer Architectures

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO full questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. Define Instruction Set Architecture (ISA). Explain seven dimensions of an ISA. **(10 Marks)**

b. Assume a disk subsystem with the following components and MTTF:
   i) 10 disks each rated at 1,000,000 – hour MTTF
   ii) 1 SCSI controller, 500,000 – hour MTTF
   iii) 1 power supply, 200,000 – hour MTTF
   iv) 1 fan, 2,00,000 hour MTTF
   v) 1 SCSI cable, 1,000,000 hour MTTF.

   Using the simplifying assumptions that the lifetimes are exponentially distributed and that failures are independent, compute the MTTF of the system as a whole. **(05 Marks)**

c. Briefly explain the Amdahl's law. **(05 Marks)**

2 a. With a neat diagram, explain the classic five stage pipeline for a RISC processor. **(08 Marks)**

b. Explain different techniques in reducing pipeline branch penalties. **(06 Marks)**

c. Consider the unpipelined processor in RISC. Assume that it has a 1ns clock cycle and that it uses 4 cycles for ALU operations and branches and 5 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40%, respectively. Suppose that due to clock skew and setup, pipelining the processor adds 0.2ns of overhead to the clock. Ignoring any latency impact, how much speedup in the instruction execution rate will be given from a pipeline? **(06 Marks)**

3 a. What are data dependencies? Mention the different types of dependencies. Explain name dependencies with example. **(06 Marks)**

b. What is the drawback of 1 bit dynamic branch prediction method? Clearly state how it is overcome in 2-bit prediction. Give the state transition diagram of 2-bit predictor. **(06 Marks)**

c. With a neat diagram, give the basic structure of Tomasulo based MIPS FP unit and explain the various field of reservation stations. **(08 Marks)**

4 a. Explain the basic VLIW approach for exploiting ILP, using multiple issues. **(08 Marks)**

b. Explain branch target buffer with neat diagram. **(04 Marks)**

c. Explain Pentium 4 pipeline supporting multiple issue with speculation. **(08 Marks)**

PART – B

5 a. Explain with a neat diagram the basic structure of a centralized shared memory and distributed shared memory multiprocessor. **(10 Marks)**

b. To achieve a speedup of 80 with 100 processors what fraction of the original computation can be sequential? **(04 Marks)**

c. Explain directory based cache coherence for a distributed memory multiprocessor system along with the state transition diagram. **(06 Marks)**

6 a. List the basic cache optimization techniques. Explain any four. **(10 Marks)**
b. With a neat diagram, explain the translation buffer of fast address translation. **(10 Marks)**

7 a. Which are the major categories of advanced optimization of cache performance? Explain any two. **(10 Marks)**
b. Explain briefly how memory protection is enforced via virtual memory and via virtual machines. **(10 Marks)**

8 a. Explain detecting and enhancing loop level parallelism for VLIW. **(10 Marks)**
b. Explain the architecture of IA64 intel processor and also the prediction and speculation support provided. **(10 Marks)**

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