CBCS SCHEME

USN | | | | | | | | | | 17CS/IS32

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Analog & Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the construction and operation principle of N-channel JFET along with its characteristic curves. **(08 Marks)**

b. The Fig. Q1 (b) shows a biasing configuration using DE-MOSFET. Given that the saturation Drain current is 8 mA and the pinch off voltage is -2 V; determine the value of Gate, source voltage, Drain current and the drain source voltage. **(06 Marks)**

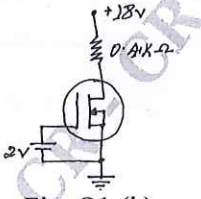

Fig. Q1 (b)

c. With neat figure and relevant waveforms, explain the working of relaxation oscillator circuit using op-amp. **(06 Marks)**

OR

2 a. Explain the working of an Astable multivibrator with necessary diagrams and expressions for frequency of oscillation, using timer IC 555. **(08 Marks)**

b. Differentiate between JFETs and MOSFETs. **(05 Marks)**

c. With neat figure, explain the operation of Peak Detector Circuit using op-amp. **(07 Marks)**

Module-2

3 a. Discuss positive and negative logic and list equivalences in positive and negative logic. **(04 Marks)**

b. A digital system is to be designed in which the months of the year is given as input in four bit form. The month January is represented as '0000', February as '0001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0'. Consider excess numbers in the input beyond '1011' as don't care conditions. For this system of four variables (A, B, C, D) find the following:

(i) Boolean expression in $\sum$m and $\prod$M form.

(ii) Using K-map simplify in SOP form.

(iii) Implement using NAND-NAND gates. **(08 Marks)**

c. Simplify, using QM method: $F(A,B,C,D) = \sum m(1,2,8,10,11,14,15)$ **(08 Marks)**

OR

4 a. What are static hazards? How to design a hazard free circuit? Explain with an example. **(08 Marks)**

b. Write a verilog code for the Fig. Q4 (b) in, (i) Structural model (ii) Dataflow model and (iii) Behavioural model. **(08 Marks)**

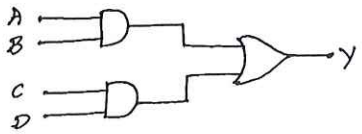

Fig. Q4 (b)

c. Prove that duty cycle of a symmetrical waveform is 50%. An asymmetrical signal waveform is high for 2 ms and low for 3 ms. Find period, frequency and duty cycle high. **(04 Marks)**

Module-3

5 a. Implement $Y(A,B,C,D) = \sum m(0,2,3,4,5,8,9,10,11,12,13,15)$ using 8 to 1 multiplexer. **(06 Marks)**

b. What is magnitude comparator? Write the truth table and logic circuit of a 1 bit comparator. **(06 Marks)**

c. What are different types of PLDs? Implement the 7 segment decoder using PLA. **(08 Marks)**

OR

6 a. Design a priority encoder for a system with three inputs; the middle bit with highest priority encoding to 10, the MSB with next priority encoding to 11, while the LSB with least priority encoding to 01. **(08 Marks)**

b. Write a verilog code for a A-to-1 multiplexer using conditional assignment statement. **(06 Marks)**

c. Differentiate combinational and sequential circuits. **(06 Marks)**

Module-4

7 a. With block diagram, truth table and waveforms, explain the working of Master-Slave JK Flip-Flop. **(07 Marks)**

b. Name and explain in short the four basic types of shift registers and draw a block diagram for each. **(08 Marks)**

c. Bring out the differences between asynchronous and synchronous counters. **(05 Marks)**

OR

8 a. What is switch contact bounce? How to remove any contact bounce due to switch using SR latch. **(08 Marks)**

b. How long it will take to shift the hexadecimal number 'AB' into 54/74164 (SIPO), if the clock is 5 MHz? **(02 Marks)**

c. Explain 4-bit sequence generator and programmable 4-bit sequence detector. **(10 Marks)**

Module-5

9 a. What do you mean by lockout condition in counters? Using JK flip-flops design self correcting mod-6 counter. **(10 Marks)**

b. What is accuracy and resolution of the D/A converter? Explain with example. What is the resolution of a 9-bit D/A converter which uses a ladder network? If the full-scale output voltage of this converter is +5 V, what is resolution in volts? **(10 Marks)**

OR

10 a. Discuss two drawbacks of resistive divider used in converting digital input to analog output. Draw the schematic for a 4-bit binary ladder and explain how digital to analog conversion is achieved using it. **(10 Marks)**

b. Explain the concept of 'successive approximation' of A/D converter. **(10 Marks)**

* * * * *