CBCS SCHEME

USN | | | | | | | | | | 18CS34

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the basic operational concepts of the computer with a neat diagram. **(06 Marks)**

b. What is performance measurement? Explain the overall SPEC rating for the computer in a program suite. **(08 Marks)**

c. Explain the following :
(i) Byte addressability (ii) Big-endian assignment (iii) Little-endian assignment. **(06 Marks)**

OR

2 a. Show how the below expression will be executed in one address, two address and three address processors in an accumulator organization.
$X = A \times B + C \times D$ **(08 Marks)**

b. What is the effective address of the source operand in each of the following instructions, when the Register R1, and R2 of computer contain the decimal value 1200 and 4600?
(i) Load 20(R1), R5 (ii) Move #3000, R5 (iii) Store R5, 30(R1, R2)
(iv) Add – (R2), R5 (v) Subtract (R1)+, R5 **(08 Marks)**

c. Interpret the Subroutine Stack Frame with example. **(04 Marks)**

Module-2

3 a. Illustrate a program that reads one line from the keyboard, stores it in memory buffer, and echoes it back to the display in an I/O interfaces. **(10 Marks)**

b. What is an interrupt? What are Interrupt service routines and what are vectored interrupts? Explain with example. **(10 Marks)**

OR

4 a. Demonstrate the DMA and its implementation and show how the data is transferred between memory and I/O devices using DMA controller. **(08 Marks)**

b. With a neat diagram, explain the general 8-bit parallel interface circuit. **(06 Marks)**

c. Explain PCI bus data transfer in a computer system. **(06 Marks)**

Module-3

5 a. Explain the organization of 1k × 1 memory chip. **(08 Marks)**

b. With a neat figure explain the direct mapped cache in mapping functions. **(08 Marks)**

c. What is memory interleaving? Explain. **(04 Marks)**

OR

6 a. With a neat diagram briefly explain the internal organization of 2M × 8 dynamic memory chip. **(08 Marks)**

b. Illustrate cache mapping techniques. **(06 Marks)**

c. Calculate the average access time experienced by a processor, if a cache hit rate is 0.88, miss penalty is 0.015 milliseconds and cache access time is 10 microseconds. **(06 Marks)**

Module-4

7 a. Perform the addition and subtraction of signed numbers:
(i) +4 and −6 (ii) −5 and −2 (iii) +7 and −3 (iv) +2 and +3 **(08 Marks)**

b. Explain 4 bit carry - look ahead adder with a neat diagram. **(06 Marks)**

c. Perform bit pair recoding for (+13) and (−6). **(06 Marks)**

OR

8 a. Perform Booth's algorithm for signed numbers (− 13) and (+ 11). **(10 Marks)**

b. Show and perform non restoring division for 3 and 8. **(10 Marks)**

Module-5

9 a. Illustrate the sequence of operations required to execute the following instructions
Add (R3), R1 **(10 Marks)**

b. Explain the three bus organization of a data path with a neat diagram. **(10 Marks)**

OR

10 a. Compare and contrast the following :
(i) Hard - wired control
(ii) Microprogrammed control. **(10 Marks)**

b. What is pipeline? Explain the 4 stages pipeline with its instruction execution steps and hardware organization. **(10 Marks)**

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