USN | | | | | | | | | | |

10EC751

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. With a neat block diagram, explain the issues to be considered in designing and implementing a DSP system. **(04 Marks)**

b. With a neat block diagram, explain the methods of sampling rate conversions in DSP system. And if the sequence x(n) = [0, 4, 8, 12, 16] is interpolated using interpolation sequence b_k = [1/4, 2/4, 3/4, 2/4, 1/4] and the interpolation factor is 4. Find the interpolated sequence y(m). **(16 Marks)**

2 a. Draw and explain 4 × 4 Braun multiplier structure. What is the total propagation delay if each adder introduces 1.4 units of delay? **(07 Marks)**

b. What is meant by circular addressing mode? Write pointer updating algorithm for the circular addressing mode and show different cases that encounter during updating process of the pointer. **(08 Marks)**

c. Explain implementation of a 16-tap FIR filter, using two MAC units (parallel). Draw its block diagram. **(05 Marks)**

3 a. Compare architectural features of TMS320C25 and ADSP2100 fixed point digital signal processor. **(06 Marks)**

b. Write an explanatory note on direct addressing mode of TMS320C54XX processor. **(10 Marks)**

c. Assuming the current contents of AR3 to be 0200h, what will be its contents after each of the following TMS320C54XX addressing modes is used? Assume that the contents of ARO is 0020h.

i) *AR3 + 0
ii) *+AR3 (40h)
iii) *AR3-
iv) *AR3

(04 Marks)

4 a. Describe with a neat block diagram, the operation of hardware timer in TMS320C54XX DSP's. **(10 Marks)**

b. Show the pipeline operation of the following sequence of instructions if the initial values of AR1, AR3, A are 84, 81, 1 and the values stored in memory location 81, 82, 83, 84 are 2, 3, 4, 6. Also provide the values of registers AR3, AR1, T and accumulator, A, after completion of each cycle.

```
ADD *AR3+, A
LD *AR1+, T
MPY *AR3+, B
ADD B, A
  ⋮
```

(10 Marks)

PART – B

5 a. Determine the value of each of the following 16-bit numbers represented using the given Q-notations:
   i) 4400h as a Q0 number
   ii) 4400h as a Q7 number
   iii) -0.3125 as a Q15 number
   iv) -352 as a Q0 number **(04 Marks)**

b. Write an assembly language program for TMS320C54XX processor to multiply two Q15 numbers to produce Q15 number result. **(06 Marks)**

c. Explain how FIR filter can be implemented using TMS320C54XX processor. **(10 Marks)**

6 a. Determine the following for a 512-point FFT computation:
   i) Number of stages
   ii) Number of butterflies in each stage
   iii) Number of butterflies needed for the entire computation
   iv) Number of butterflies that needed no twiddle factors
   v) Number of butterflies that require real twiddle factors
   vi) Number of butterflies that require complex twiddle factors. **(06 Marks)**

b. Explain how scaling prevents overflow condition in the butterfly computation. Derive the optimum scaling factor for the DIT-FFT butterfly. **(10 Marks)**

c. Write the structure of an 8-point DIT-FFT implementation. Take scaling factor for all butterflies as (1/4). **(04 Marks)**

7 a. Design a data memory system with address range 000800h – 000FFFh for a C5416 processor using 2k × 8 SRAM memory chips. **(06 Marks)**

b. Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode. **(06 Marks)**

c. Describe DMA with respect to TMS320C54XX processors. **(08 Marks)**

8 a. Explain PCM3002 CODEC, with the help of a neat block diagram. **(10 Marks)**

b. With the help of a block diagram, explain the image compression and reconstruction using JPEG encoder and decoder. **(10 Marks)**

* * * * *