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10TE74

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain the issues to be considered in designing and implementing a DSP system. **(06 Marks)**

b. The sequence x(n) = [0 2 4 6 8] is interpolated using an interpolation filter b_k = [0.5 1 0.5] with interpolation factor 2. Determine the interpolation sequence. **(06 Marks)**

c. Explain a digital signal processing system with the help of a block diagram. **(08 Marks)**

2 a. Suggest a scheme to implement a multiplier to multiply two unsigned number using 4×4 Braun multiplier as the building block. **(06 Marks)**

b. What is meant by circular addressing mode? Write pointer updated algorithm for the circular addressing mode and show different cases that encounter during the updating process of the pointer. **(06 Marks)**

c. Draw the block diagram to implement 8-tap FIR filter using (i) 8 MAC unit (ii) 2 MAC unit and compare the performance. **(08 Marks)**

3 a. With a help of functional diagram, explain about Multiplier / Adder unit of TMS320C54XX processor. **(06 Marks)**

b. With the block diagram explain the direct addressing mode of TMS320C54XX processor. **(06 Marks)**

c. Explain the PMST register. **(08 Marks)**

4 a. Describe the operation of the following instrumentations of TMS320C54XX processors with an example:
(i) MPY #01234, A (ii) MPY *AR2–, *AR4 + 0, B
(iii) MAC *AR5+, #1234h, A (iv) MAS $*AR_3^-$, $*AR_4$ +, B **(08 Marks)**

b. Explain the six stages pipelined execution of TMS320C54XX processor. **(06 Marks)**

c. Write an ALP of TMS320C54XX process to compute sum of three product terms given by the equation y(n) = h(0)x(n) + h(1) x(n – 1) + h(2) x(n – 2) using direct addressing mode where h(0), h(1) and h(2) are stored in data memory location h and x(n), x(n – 1) and x(n – 2) are stored in data memory location x. y(n) is saved in data memory location y and y + 1. **(06 Marks)**

PART – B

5 a. Represent each of the following as 16-bit numbers in the desired Q-notation
(i) 0.35 in Q_{15} (ii) – 0.1958 in Q_{15} (iii) 4000h in Q_{15} (iv) 4000h in Q_7 **(06 Marks)**

b. Write a TMS320C54XX program that illustrate the multiplication of two Q_{15} number to produce Q_{15} result. Write comments. **(06 Marks)**

c. Write an ALP to implement FIR filter. **(08 Marks)**

6 a. Explain how scaling prevents overflow condition in the butterfly computation. Draw the optimum scaling factor for the DIT-FFT butterfly. **(10 Marks)**

b. Explain how the bit reversal index generation can be done in 8-point FFT. Also write a TMS320C54XX subroutine program for 8 point DITFFT bit reversal index generation with comment. **(10 Marks)**

7 a. Draw the memory interface signals for a read-read-write sequence of operations and also explain the signals that are involved. **(06 Marks)**

b. Describe DMA with respect to TMS320C54XX processor. **(08 Marks)**

c. Draw the flow chart of the interrupt handling by the C54XX processor and explain. **(06 Marks)**

8 a. Explain with a neat diagram the operation of the pitch detector. **(10 Marks)**

b. Draw the block diagram of JPEG encoder and decoder and also explain how JPEG encoding and decoding is implemented in DSP. **(10 Marks)**

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