CBCS SCHEME

USN | | | | | | | | | | |

15EC53

Fifth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Verilog HDL

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the advantages of HDL's over schematic-based design. **(06 Marks)**
b. Explain top-down design methodology and bottom-up design methodology. **(10 Marks)**

OR

2 a. Discuss the trends in HDLs. **(06 Marks)**
b. Explain the design hierarchy using 4-bit ripple carry counter. **(10 Marks)**

Module-2

3 a. Explain the following data types with an example in verilog:
i) Vectors ii) Registers iii) Time iv) Real. **(08 Marks)**
b. What are system tasks and compiler directives? Explain. **(08 Marks)**

OR

4 a. What are the components of SR-latch? Write verilog HDL module of SR-latch. **(08 Marks)**
b. With an example, explain Hierarchical names. **(08 Marks)**

Module-3

5 a. With the help of logic diagram, write a verilog code for 4 to 1 multiplexer using gate – level modeling. **(08 Marks)**
b. What are rise, fall and turn-off delays? Explain, how they are specified in verilog. **(08 Marks)**

OR

6 a. Explain conditional and concatenation operator with an example. **(06 Marks)**
b. Write a verilog dataflow description for 4-bit full adder with carry lookahead. **(10 Marks)**

Module-4

7 a. Explain briefly event based timing control in verilog. **(08 Marks)**
b. Explain sequential and parallel blocks of verilog HDL. **(08 Marks)**

OR

8 a. Write a verilog HDL code for JK flip-flop using case statement. **(08 Marks)**
b. With syntax, explain conditional and branching loop statements in verilog HDL. **(08 Marks)**

Module-5

9 a. Explain the advantages and benefits of VHDL. **(06 Marks)**
b. Write a VHDL code for full-adder using two half adder in mixed style description. **(10 Marks)**

OR

10 a. Explain the synthesis process with a block diagram. **(10 Marks)**
b. Differentiate between signal assignment and variable assignment. **(06 Marks)**

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