CBCS SCHEME

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15TE73

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020
CMOS VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the DC transfer characteristics of complementary CMOS inverter and mark all the regions of operation with necessary expressions for V_{out} in each region. **(07 Marks)**

b. Describe with neat diagram, the P-well fabrication process. **(06 Marks)**

c. Compare CMOS and Bipolar technology. **(03 Marks)**

OR

2 a. Explain nMOS fabrication process. **(07 Marks)**

b. Discuss :
i) Channel length modulation
ii) Body effect. **(06 Marks)**

c. Demonstrate the operation of tristate inverter with neat diagram. **(03 Marks)**

Module-2

3 a. Explain 'λ' based design rules for wires (nMOS and CMOS). **(08 Marks)**

b. Draw the stick diagram/layout for the nMOS implementation of the Boolean function $\overline{X} = A + BC$. **(08 Marks)**

OR

4 a. Define sheet resistance 'R_S' and standard unit of capacitance $\square C_g$. Estimate the value of capacitance in $\square C_g$ for the given metal layer shown in Fig.Q4(a), if features size is $2\lambda \times 2\lambda$ and relative value of metal to substrate = 0.075. **(04 Marks)**

Fig.Q4(a)

b. Estimate rise-time and fall time for CMOS inverter. **(06 Marks)**

c. Explain inverting and non-inverting type nMOS super buffer. **(06 Marks)**

Module-3

5 a. Determine the scaling factors for the following :
i) Gate capacitance 'C_g'
ii) Gate delay 'T_d'
iii) Saturation current 'Id_{ss}'
iv) Current density 'J'. **(08 Marks)**

b. Explain the design of 4 bit shifter using 4 × 4 crossbar switch. **(08 Marks)**

OR

6 a. Explain 4 bit data path for processor with neat block diagram. **(04 Marks)**

b. Explain Manchester carry chain. **(04 Marks)**

c. Explain Carry LookAhead Adder (CLA) and represent the 4 bit block CLA unit. **(08 Marks)**

Module-4

7 a. Discuss the architectural issues related to sub-system design. **(04 Marks)**

b. Explain the structured design of a parity generator with necessary blocks and stick diagram. **(08 Marks)**

c. Explain switch logic of a 4 – way multiplexer for nMOS switches. **(04 Marks)**

OR

8 a. Explain pseudo – nMOS logic for NAND gate and inverter. **(04 Marks)**

b. Explain in detail the generic structure of an FPGA. **(06 Marks)**

c. Discuss goals and techniques of FPGA. **(06 Marks)**

Module-5

9 a. What are timing considerations in system design? **(04 Marks)**

b. Explain the working of 3 transistor dynamic RAM cell. **(07 Marks)**

c. Explain observability and controllability in testing. **(05 Marks)**

OR

10 a. Explain CMOS pseudo static D-flip-flop circuit. **(06 Marks)**

b. Discuss the following :

i) Ad–hoc testing

ii) IDDQ testing. **(10 Marks)**

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