CBCS SCHEME

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15EC63

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the step-by-step CMOS P-Well fabrication process. **(08 Marks)**

b. With the mathematical equations, explain velocity saturation and mobility degradation effect due to increase in saturation current. **(08 Marks)**

OR

2 a. With the transfer characteristic of skewed inverter, explain the beta ratio effects. **(06 Marks)**

b. Compare CMOS and bipolar technologies. **(06 Marks)**

c. Consider the nMOS transistor in a 180 nm process with a nominal threshold of 0.4V and doping level of 8×10^{17} cm^{-3}. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 1.1V instead of '0'? **(04 Marks)**

Module-2

3 a. Discuss the λ-based design rules (i) Butting contact (ii) Transistors (nMOS, pMOS and CMOS) **(08 Marks)**

b. Derive the expression of delay interms of τ for CMOS inverter pair. **(08 Marks)**

OR

4 a. Draw the layout for $\overline{Y} = A + BC$ using CMOS. **(08 Marks)**

b. Find the C_{in} for the layout shown in Fig.Q4(b).

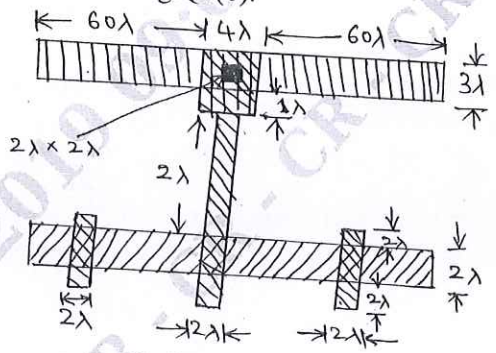

Fig.Q4(b)

Module-3

5 a. Define scaling. Explain the scaling factors for device parameters. **(08 Marks)**

b. What is Manchester Carry Chain? Explain it. **(08 Marks)**

OR

6 a. What are the problems associated with VLSI design and how to reduce by using standard practice? **(06 Marks)**

b. Draw the 4 × 4 cross bar switch using MOS switches and explain it. **(06 Marks)**

c. Calculate the Regularity for 4 × 4 bit and 8 × 8 bit shifter. **(04 Marks)**

Module-4

7 a. Construct a stick diagram for an nMOS parity generator as shown in Fig.Q7(a). The required response is such that z = 1 if there is an even number (including zero) of 1s on the input and z = 0 if there is an odd number.

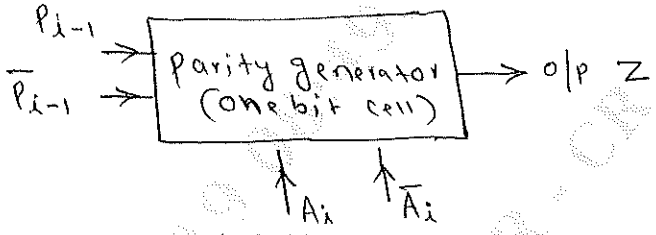

Fig.Q7(a) **(08 Marks)**

b. Draw the block diagram of Generic structure of an FPGA fabric and explain it. **(08 Marks)**

OR

8 a. Construct a stick diagram for an multiplexer shown in Fig.Q8(a) using CMOS.

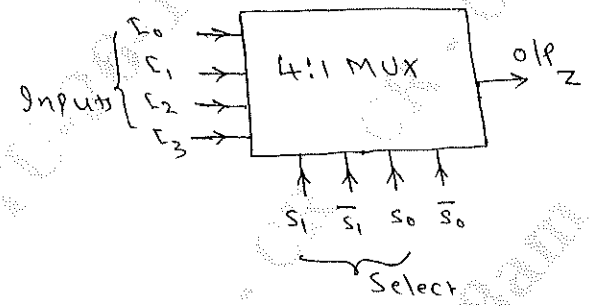

Fig.Q8(a) **(08 Marks)**

b. Explain the goals and techniques of FPGA based system design. **(08 Marks)**

Module-5

9 a. What are the requirements for system timing considerations? **(06 Marks)**

b. Explain the operation of a three transistor dynamic RAM cell. **(06 Marks)**

c. Write a note on stuck - at faults. **(04 Marks)**

OR

10 a. With the help of block diagram, explain the process of logic verification. **(08 Marks)**

b. Explain the operation of CMOS pseudo-static memory cell. **(08 Marks)**

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