

CBCS SCHEME



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17EC33

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020 Analog Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1.
 - a. Derive the expression for input impedance, output impedance, voltage gain and current gain for common emitter voltage divider bias configuration using re model. (10 Marks)
 - b. For the emitter-follower circuit shown in Fig.Q.1(b). Determine:
 - i) Input impedance
 - ii) Output resistance
 - iii) Voltage gain
 - iv) Current gain.

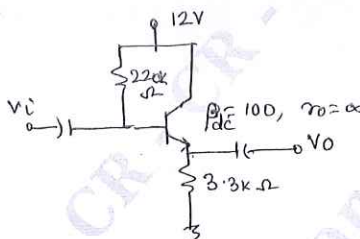


Fig.Q.1(b)

(10 Marks)

OR

2.
 - a. Derive the expression for voltage gain, current gain, input resistance, output resistance CE transistor amplifier using hybrid parameters. (10 Marks)
 - b. Describe the hybrid π -model. (04 Marks)
 - c. Determine Z_i , Z_o , A_v , A_i for the circuit shown in Fig.Q.2(c) using approximate hybrid model. (06 Marks)

Given data $h_{ie} = 1.1K\Omega$, $h_{fe} = 100$, $h_{oe} = 20\mu A/V$

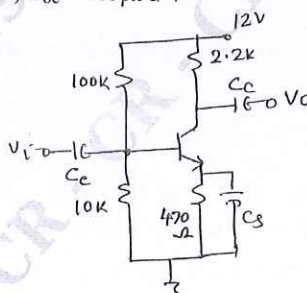


Fig.Q.2(c)

Module-2

3.
 - a. Indicate various operating regions of JFET. Also determine parameters from the characteristics. (06 Marks)
 - b. Analyze self bias configuration of JFET and derive the expression for voltage gain, output impedance and input impedance. (07 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

- c. Compute g_m , z_i , z_o and A_v for the circuit shown in Fig.Q.3(c). Given $V_{GSQ} = -2.2V$, $I_{DQ} = 2.03mA$, $I_{DSS} = 10mA$, $V_p = -4V$ and $r_d = 40K\Omega$. (07 Marks)

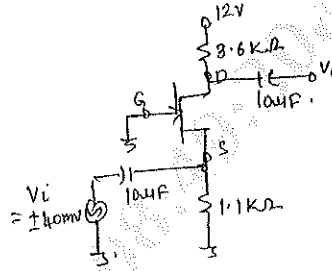


Fig.Q.3(c)

OR

- 4 a. Explain the characteristics of enhancement type MOSFET. Also indicate various operating regions. (06 Marks)
 b. Derive the expression voltage gain, input resistance and output resistance of the source follower. (07 Marks)
 c. Evaluate z_i , z_o and A_v for the JFET circuit shown in Fig.Q.4(c). Given: $I_{DSS} = 12mA$, $V_p = -3V$, $g_m = 2m\Omega$, $r_d = 40K\Omega$ (07 Marks)

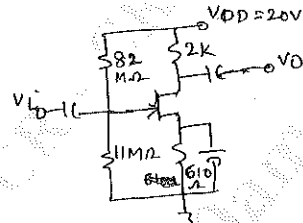


Fig.Q.4(c)

Module-3

- 5 a. Derive the expression for cut-off frequency due to source capacitor and coupling capacitor of a BJT amplifier. (06 Marks)
 b. If the applied ac power to a system is $5\mu W$ at $100mV$ and the output power is $48W$, Determine: i) Power gain in dB ii) The voltage gain in dB if the output impedance is $40K\Omega$ iii) The input impedance. (06 Marks)
 c. Derive an expression for Miller input and output capacitance. Also draw the equivalent circuit. (08 Marks)

OR

- 6 a. Derive the expression f'_L and f'_H for the multistage amplifier. (06 Marks)
 b. For the circuit shown in Fig.Q.6(b) determine f_{Hi} and f_{Ho} , given $C_{wi} = 3pF$, $C_{wo} = 5pF$, $C_{gd} = 4pF$, $C_{gs} = 6pF$, $C_{ds} = 1pF$, $I_{DSS} = 6mA$, $V_p = -6V$ $r_d = \infty$ and $g_m = 2m\Omega$. (08 Marks)

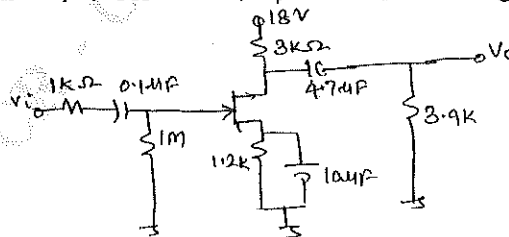


Fig.Q.6(b)

- c. Determine overall lower 3dB and upper 3dB frequency for a four stage amplifier having an individual value of $f_1 = 40\text{Hz}$ and $f_2 = 2.5\text{MHz}$. Also calculate overall bandwidth. (06 Marks)

Module-4

- 7 a. Explain the concept of feed back using block diagram. (06 Marks)
 b. Derive the expression for input resistance and output resistance of a voltage series feedback amplifier. (08 Marks)
 c. If the gain of an amplifier changes from a value of -1000 by 10%, calculate the gain change, if the amplifier used in a feedback circuit having $\beta = \frac{-1}{20}$. (06 Marks)

OR

- 8 a. Explain the operation of FET phase shift oscillator. (08 Marks)
 b. Describe the Wein bridge oscillator for the oscillating frequency $f_0 = 2.2\text{kHz}$. Also draw the circuit diagram. (06 Marks)
 c. Determine the oscillating frequency of the Colpitts oscillator for the given specifications $C_1 = 750\text{pF}$, $C_2 = 2500\text{pF}$ and $L = 40\mu\text{H}$. Also calculate the feedback factor of the Colpitts oscillator. (06 Marks)

Module-5

- 9 a. Derive an expression for conversion efficiency of transformer coupled class-A amplifier. (08 Marks)
 b. Calculate the second harmonic distortion for an output waveform having measured values of $V_{CEmin} = 2.4\text{V}$, $V_{CEQ} = 10\text{V}$ and $V_{CEmax} = 20\text{V}$. (04 Marks)
 c. Explain with the help of neat circuit diagram, voltage series regulator operation. (08 Marks)

OR

- 10 a. Derive an expression for conversion efficiency of class B push pull amplifier. (08 Marks)
 b. A transformer coupled class-A amplifier drives a 16Ω speaker through 4:1 transformer using a power supply of $V_{cc} = 36\text{V}$, the circuit delivers 2W to the load. Calculate : i) $P(ac)$ across transformer primary ii) $V_L(ac)$. (06 Marks)
 c. Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.1V, second harmonic component amplitude of 0.3V, third harmonic component of 0.1V and fourth harmonic component of 0.05V. Also calculate total harmonic distortion. (06 Marks)

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