CBCS SCHEME

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15EE34

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain the dc analysis of emitter stabilized bias circuit. State its advantages and disadvantages. **(06 Marks)**

b. Obtain an expression for S_{VBE} OR S′ for voltage divider bias circuit. Also express relation between S_{ICO} (S) and S_{VBE} (S′). **(10 Marks)**

OR

2 a. For voltage divider bias circuit R_1 = 68KΩ, R_2 = 6.8KΩ, R_C = 3.3KΩ, R_E = 1KΩ, V_{CC} = 12V and β = 100. Determine the location of Q-point. Draw the circuit diagram. **(10 Marks)**

b. For the circuit shown in Fig.Q.2(b), determine V_{CE}, VE and IE. Given that R_B = 220KΩ, R_E = 2.2KΩ, V_{BB} = 5V, V_{EE} = -5V, β = 100. **(06 Marks)**

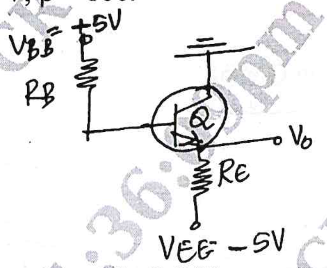

Fig.Q.2(b)

Module-2

3 a. State the conditions to operate transistor in saturation region, just out of saturation region and for active region. **(03 Marks)**

b. For the common collector circuit shown in Fig.Q.3(b), R_1 = 47KΩ, R_2 = 4.7KΩ, R_E = 3.3KΩ, R_L = 10KΩ, R_S = 1KΩ, hic = 1.2KΩ, h_{fc} = -101, hrc = 1 and hoc = 25μA/V. Determine A_I, Z_i, Av and Avs. How do you justify your results? Use exact h-parameter model. **(10 Marks)**

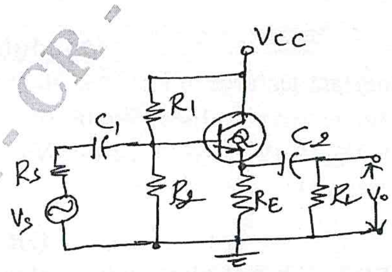

Fig.Q.3(b)

c. State and explain the conditions to apply approximate h-parameter model for small signal equivalent circuit. **(03 Marks)**

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OR

4 a. Consider a hybrid II model for CE stage. Explain the variation of current gain vs frequency. Obtain an expression for cut off frequency f_β. **(10 Marks)**

b. The short circuit CE current gain of transistor is 50 at a frequency of 5MHZ, if f_β = 300kHz, determine f_T, hfe and /Ai/ when f = 10MHZ. **(06 Marks)**

Module-3

5 a. For the 2-stage cascade amplifier shown in Fig.Q.5(a), calculate A_I, A_V, Z_i, Z_o. Given h_{ie} = 1.1KΩ, h_{fe} = 50, h_{re} = h_{oe} = 0. **(10 Marks)**

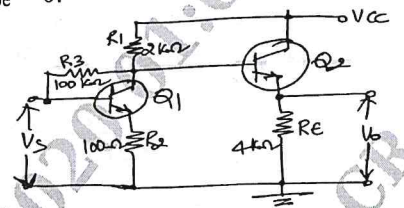

Fig.Q.5(a)

b. What is a CASCODE amplifier? Draw the circuit of CASCODE amplifier. State its advantage. **(06 Marks)**

OR

6 a. Obtain an expression for transfer gain and stability of gain in negative feedback amplifier. **(08 Marks)**

b. For the voltage series feedback amplifier shown in Fig.Q.6(b), calculate D, A_{vf}, Z_{if} and Z'_{of}. **(08 Marks)**

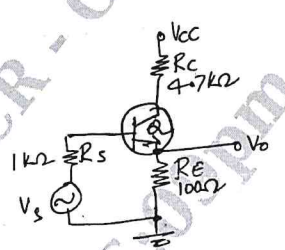

Fig.Q.6(b)

Module-4

7 a. Derive an expression for second harmonic distortion and power output due to distortion in a power amplifier. Use 3-point method. **(10 Marks)**

b. A complementary push pull amplifier has capacitive couple load, R_L = 8Ω, V_{CC} = ±12V, find $P_{ac\,max}$, P_D of each transistor and conversion efficiency. **(06 Marks)**

OR

8 a. Obtain an expression for frequency of oscillations in Hartley oscillator. **(10 Marks)**

b. A crystal has α = 0.1H, C = 0.01pF, R = 10KΩ, C_M = 1pF. Find fs and Q-factor. Also state Barkhausen criteria for sustained oscillations. **(06 Marks)**

Module-5

9 a. List the important features of FET and state its drawback also. **(06 Marks)**

b. For the voltage divider bias circuit of FET, R_D = 1.2KΩ, R_S = 2KΩ, R_1 = 20KΩ, R_2 = 10KΩ, V_{DD} = 12V, I_{DSS} = 12mA, V_P = -4V, determine I_D, V_{GS}, V_G, V_{DS} and V_S. Draw the circuit diagram. **(10 Marks)**

OR

10 a. Consider JFET with self bias having unbypassed R_S. Obtain expression for Z_i Z_o and A_v. Draw the circuit diagram and small signal circuit also. **(10 Marks)**

b. Explain the differences between depletion type and enhancement type MOSFETS. **(06 Marks)**

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