CBCS SCHEME

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15EE35

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: *Answer FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Simplify the following expression using K-map. Implement the simplified expression using only NOR Gates. **(06 Marks)**

$f(a,b,c,d) = \pi M(0,3,4,7,8,10,12,14) + \sum dc(2,6)$

b. Write a short note on combinational logic circuit. **(04 Marks)**

c. Using Quine-McClusky method and prime implicant reduction, obtain minimal POS for $f(x,y,z) = \sum m(0,1,2,5,6,7) + dc(3)$ **(06 Marks)**

OR

2 a. Write a short note on MEV technique. **(04 Marks)**

b. Generate switching function for odd parity generator where input variables are a, b, c and d. Also define parity. **(06 Marks)**

c. Minimize the function using c and d as MEV on K-map.

$f(a,b,c,d) = \sum m(2,3,4,5,13,15) + d(8,9,10,11)$ **(06 Marks)**

Module-2

3 a. With a neat block diagram, explain the 4-bit carry look ahead adder. **(08 Marks)**

b. Implement the following function pairs using a 3 : 8 line decoder. $f_1(a,b,c) = \sum m(0,2,4,6)$

$f_2(a,b,c) = \sum m(1,2,4,5,7)$. **(04 Marks)**

c. Write a short note on priority encoder. **(04 Marks)**

OR

4 a. Write a short note on 2-bit binary comparator. **(04 Marks)**

b. What is a Mux Tree? Implement a 16 : 1 MUX using only 4 : 1 MUXs. **(06 Marks)**

c. Implement $f(a,b,c,d) = \sum m(0,1,5,6,7,9,10,15)$ using a 4 : 1 MUX with a and b as select lines. **(06 Marks)**

Module-3

5 a. Compare synchronous and asynchronous sequential circuits. **(04 Marks)**

b. Briefly explain the working of a Master Slave JK Flip-Flop. **(06 Marks)**

c. With neat timing diagram, explain the working of an asyncrhronous 4 bit down counter using JK Flip-Flop. **(06 Marks)**

OR

6 a. Design a mod-6 UP counter using synchronously clocked SR Flip Flops. **(08 Marks)**

b. Discuss about counters based on shift registers. **(04 Marks)**

c. With neat timing diagram, explain briefly negative edge triggered T-Flip-Flop. **(04 Marks)**

Module-4

7 a. With block diagrams, explain Melay and Moore models. (06 Marks)

b. A sequential circuit with two DFFS : A and B and input X and output Y is specified by the following next state and output equations:

$A(t+1) = AX + BX$

$B(t+1) = \overline{A}X$

$Y = (A+B)\overline{X}$

(i) Draw the logic diagram of the circuit.
(ii) Derive state table.
(iii) Derive the state diagram. (10 Marks)

OR

8 a. Explain the following state machine notations:
(i) State and state variable.
(ii) Present state and Next state.
(iii) State diagram.
(iv) State table. (04 Marks)

b. Design a sequence detector to detect the following sequence using DFF by using Melay machine.
Sequence : 1101 (12 Marks)

Module-5

9 a. Compare VHDL and Verilog. (04 Marks)

b. List all relational operators in VHDL and Verilog. (04 Marks)

c. Explain a 2×2 unsigned combinational array multiplier and write verilog description for the same. (08 Marks)

OR

10 a. List all the mathematical operators in verilog. (04 Marks)

b. Discuss about various modeling style or types of descriptions. With full adder as an example, write VHDL behavioral description. (06 Marks)

c. Explain data type vectors. For a D latch. Write verilog description. (06 Marks)

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