CMR INSTITUTE OF TECHNOLOGY

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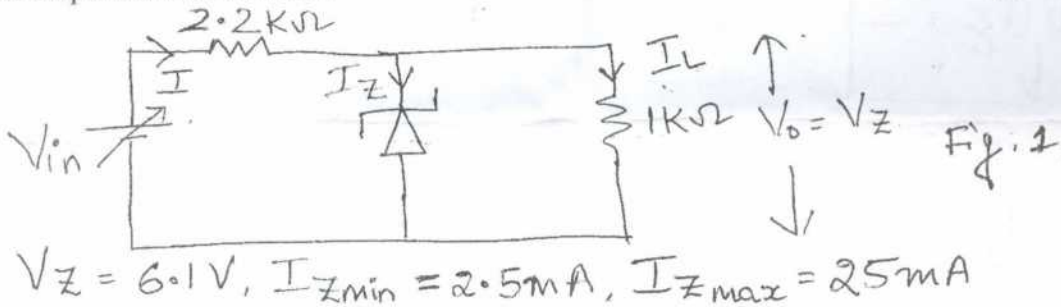
Internal Assesment Test – 2

Sub: Basic Electronics				Code: 17ELN25
Date: 17/04/2018	Duration: 90 mins	Max Marks: 50	Sem: II	Sections:- I,J,K,L,M,N,O

Answer any FIVE FULL questions.

	Marks	OBE CO	OBE RBT
1.a) For the fixed bias circuit with $\beta = 120$, draw the dc load line and determine the operating point, when $V_{CC} = 18V$, $R_B = 450k\Omega$ and $R_C = 2k\Omega$. Find V_{CEQ} & I_{CQ}.	[5]	CO2	L2,L3
b) Explain Zener diode as source and load voltage regulator circuit.	[5]		
2. a) What is DC Load Line for transistor. Explain Base Bias Circuit with necessary equations.	[5]	CO2	L2,L3
b) For a zener regulator as shown in given fig.1 Calculate the range of input voltage for output remains constant.	[5]		



3. (a)Explain the working of Half Wave Rectifier with Capacitor filter. Draw the Input and output Waveforms.	[4]	CO2	L2
(b)Explain briefly the CE circuit and sketch the input and output characteristics. Also explain operating regions by indicating them on characteristics curve.	[6]		
		CO2	L2
4. Explain the working of Full wave bridge rectifier with necessary circuit diagrams waveforms. Derive the expression for Average dc current and Efficiency for FWR.	[10]	CO2	L3
5. (a) Show that CE mode transistor acts as a voltage amplifier.	[5]		
(b) Derive the relation between α, β. Calculate α and β for the transistor if collector current is measured as 1 mA and base current is 25μA.	[5]		

6. The input voltage applied to the primary of a 4: 1 step down transformer of a full wave centre tap rectifier is 230 V; 50 Hz if the load resistance is 600Ω and forward resistance is 20Ω. Determine the following for the circuit shown in Fig.2

i) DC power output

ii) Rectification efficiency

iii) PIV

iv)ripple factor

v)ripple frequency

[10]

CO2	L3

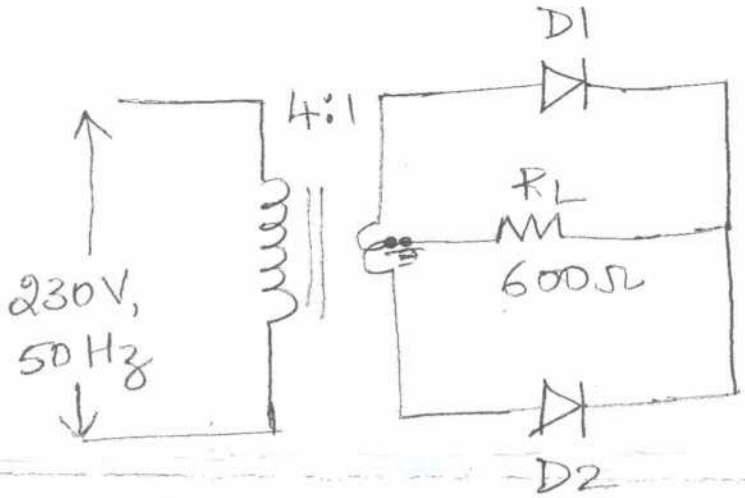


Fig. 2

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Exam Date-17/4/2018 IAT-2 Batch - (Jan - June) 2018

Marking Scheme (Basic Electronics)

Q.1 (a) ckt diagram - 1 mark
dc load line - 1 mark
Q. Point Marking - 1 mark
V_{CEQ} & I_{CEQ} — (1) + (1) Mark
} (5) Mark

(b) Source Circuit and Explanation (1) + (1.5) Mark
Load Circuit + Explanation (1) + (1.5) Mark

Q.2 (a) DC load line — (1) Mark
Base Bias ckt — (1) Mark
Explanation + Eqn's — (1) + (2) Marks
} (5) marks

(b) Calculation I_L = (1) Mark
" I_{smax} = (1) Mark
" I_{smin} = (1) "
" $V_{in\,max}$ = (1) "
" $V_{in\,min}$ = (1) "
} (5) Mark.

Q.3 (a) Working circuit — (2) Mark
— (1) Mark
I/P & O/P Wave — (1) Mark
} (4) Mark.

(b) CE ckt + characteristics + charact. O/P + Explanation
(1) Mark (1) (1) (3)

Q.4 ckt → (1) M, Working - (2), Waveform - (2)
I_{dc} - (2.5) M, Efficiency derive - (2.5) M
} Total 10 Mark

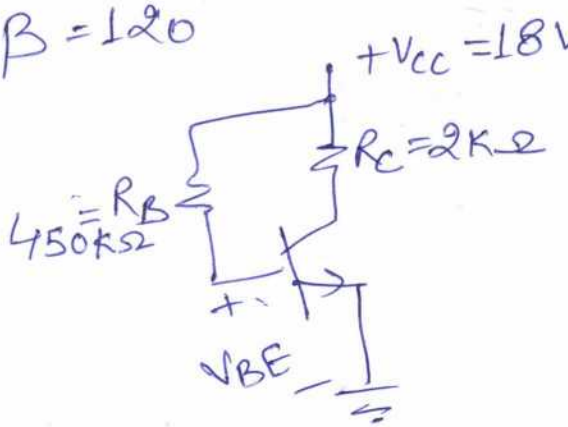
Q.5 (a) ckt → (1) M, Explanation - 4 (M)
(b) Relation α, β (3.0) Mark, α Calculation (2.0)
β Calculation (1.0)

Q.6 All parts (2) mark each
} Total 10 mark.

Q.1

(a). Given

$\beta = 120$



$V_{CEQ} = ?$

$I_{CQ} = ?$

DC load line = ?

Mark Q Point = ?

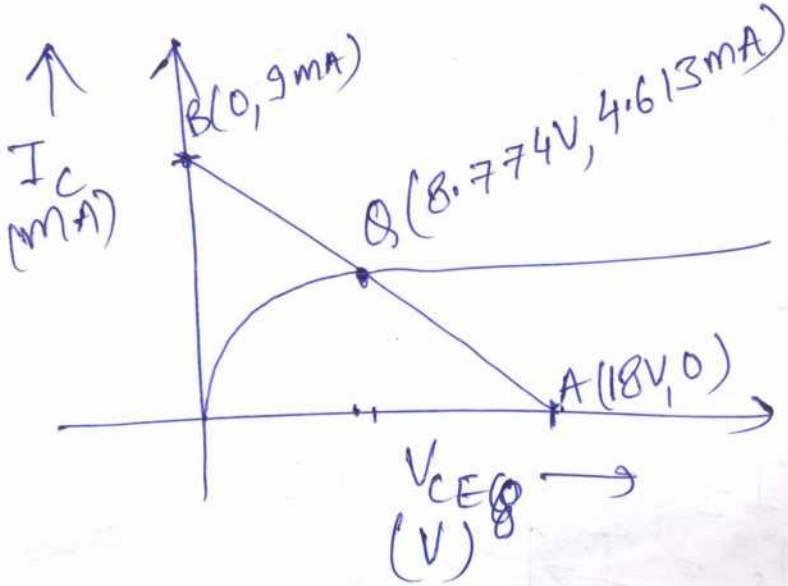
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18 - 0.7}{450 \times 10^3} = 38.44\,\mu A$$

$$I_{CQ} = \beta I_B = 120 \times 38.44 \times 10^{-6} = 4.613\,mA$$

$$V_{CEQ} = V_{CC} - I_C R_C = 18 - 4.613 \times 10^{-3} \times 2 \times 10^3$$

$$= 8.774\,V$$

So, Q (8.774 V, 4.613 mA)



For DC load line, KVL $V_{CC} = I_C R_C + V_{CE}$

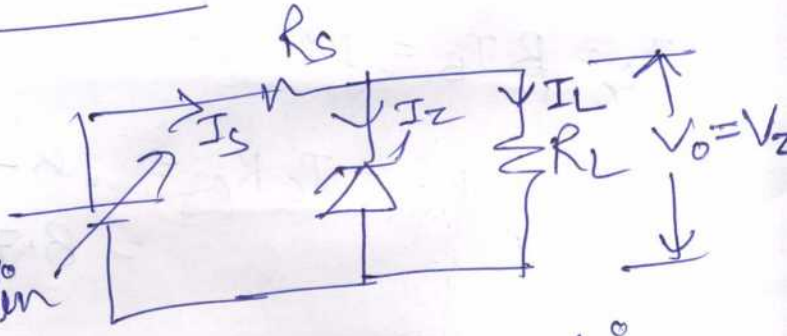
Put $I_C = 0 \Rightarrow V_{CE} = V_{CC} = 18V$

$\nearrow (18V, 0)$

Put $V_{CE} = 0 \Rightarrow I_C = \frac{V_{CC}}{R_C} = \frac{18}{2 \times 10^3} = 9mA$

Q.1(b) Zener diode is used for voltage Regulator circuit.

Source Regulator Circuit



→ When V_{in} (source) is increasing then I_S will also increase

→ If I_S increases so, we have equation

$$I_S = I_Z + I_L \quad \text{—(1)}$$

→ In order to have V_o constant ie

$V_o = I_L R_L$

I_L has to be constant since R_L is con

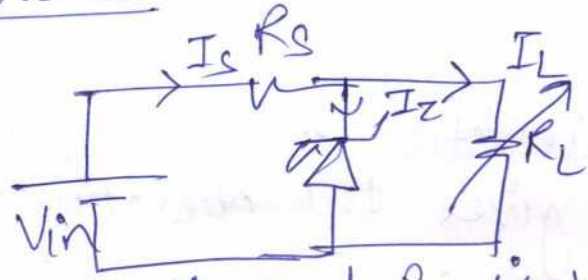
→ In eqn (1) I_S is increasing I_L is is cons

so I_Z has to increase.

$\uparrow I_S = I_Z \uparrow + I_L$ const.

→ Similarly when Vin decreases ⇒ I_S will decrease and since R_L and I_L are const. so, I_Z has to decreases.

Load Regulator Circuit



here

$$I_S = I_Z + I_L$$

Vin (source) is constant and R_L is varying.

$$V_o = I_L R_L$$

(1) when R_L increases, I_L has to decrease in order to keep V_o to be constant.

I_S is constant as Vin is constant.
I_L is decreasing
so, I_Z has to increase

$$I_S = I_Z + I_L$$
$$\text{const} \quad \text{Increase} \quad \text{decreasing}$$

(2) When R_L decreases, I_L has to increase in order to have V_o to be constant.

$$I_S = I_Z + I_L$$
$$\text{const.} \quad \text{decrease} \quad \text{increasing}$$

so, I_Z has to decrease.

Q.2(a) DC Load line for Transistor

DC load line for Transistor is drawn on the output characteristics of the Transistor.
It gives all the values of current and voltages possible for a transistor.

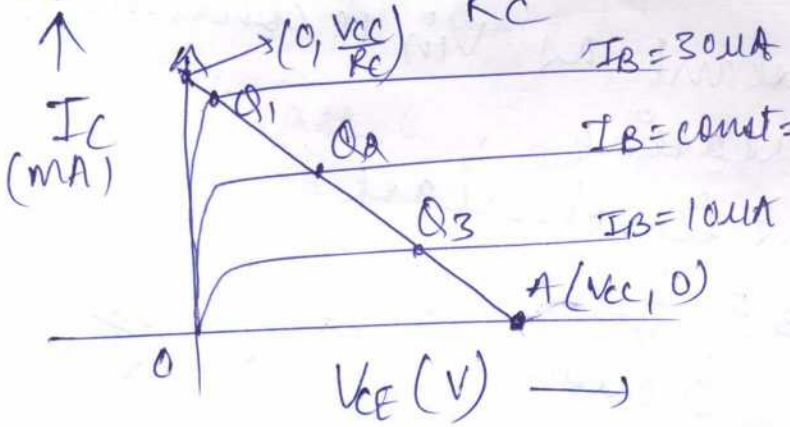
→ When this straight line cuts with output characteristic curve of transistor, the intersect point gives the operating or Q-Point.

For obtaining dc load line apply KVL at O/P side of Transistor for a CE circuit.

$$V_{CC} = I_C R_C + V_{CE}$$

Put $I_C = 0 \Rightarrow V_{CE} = V_{CC}$ $\quad A(V_{CC}, 0)$

Put $V_{CE} = 0 \Rightarrow I_C = \frac{V_{CC}}{R_C}$ $\quad B(0, \frac{V_{CC}}{R_C})$



Base Bias Circuit

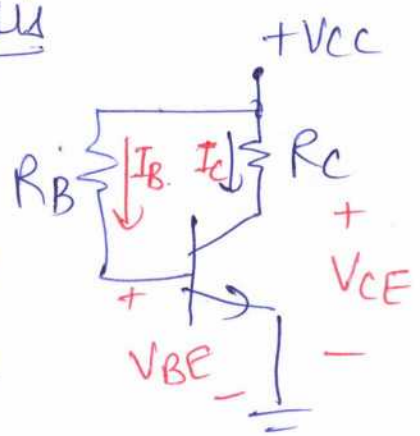
This is one of the biasing circuit used to stabilize the dc. bias or operating or Q-Point of Transistor.

Biasing circuits are mainly used improve the stability of circuit ie to stabilize the dc bias point.

→ Base bias circuit provides less stability as compared to other biasing circuit (eg. voltage divider bias). means as β of transistor changes, Q point will change.

circuit Analysis

Both Base and ~~Emit~~ Collector are provided by the supply Vcc.



Applying KVL, we have (at input side)

$$V_{CC} = I_B R_B + V_{BE}$$

$$\Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \quad — (1)$$

$\Rightarrow$ We have $\boxed{I_C = \beta I_B}$ — (2)

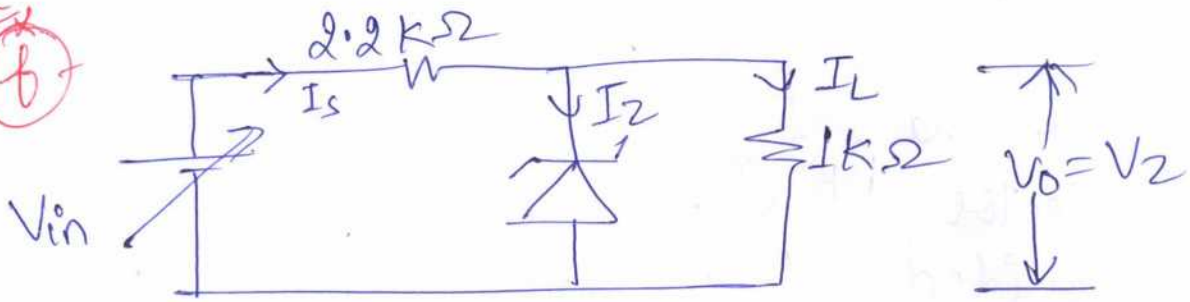
Applying KVL at output side ie across collector & emitter side,

$$V_{CC} = I_C R_C + V_{CE}$$

$$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C R_C} \quad \text{— (3)}$$

so, eqn (2) and (3) gives output current and output voltage that exists in the circuit.

Q.2 (b)



Given $V_Z = 6.1V$, $I_{Zmin} = 2.5mA$, $I_{Zmax} = 25mA$.

V_{in} Range = ?

$\rightarrow V_o = I_L R_L \Rightarrow 6.1 = I_L (1000) \Rightarrow \boxed{I_L = 6.1mA}$

$\rightarrow I_{s_{max}} = I_{Z_{max}} + I_L = 25 + 6.1 = 31.1mA$

$\rightarrow I_{smin} = I_{Zmin} + I_L = 2.5 + 6.1 = 8.6mA$

$\rightarrow V_{in_{max}} = I_{s_{max}} R_s + V_Z = 31.1 \times 10^{-3} \times 2.2 \times 10^3 + 6.1 = 74.52V$

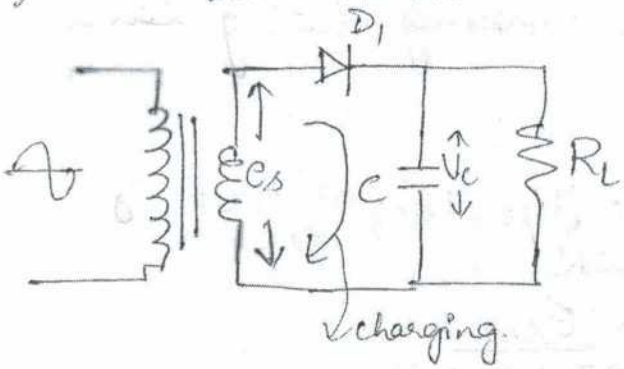
$\rightarrow V_{in\,min} = I_{smin} R_s + V_Z = 8.6 \times 10^{-3} \times 2.2 \times 10^3 + 6.1$
$= 25.02V$

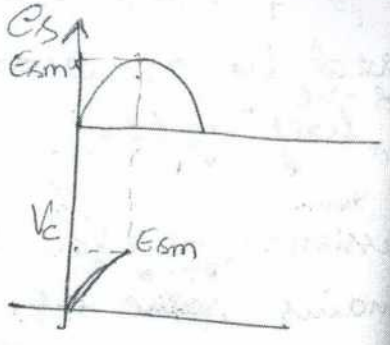
So, Range of V_{in} is 25.02V to 74.52V

$\boxed{25.02V < V_{in} < 74.52V}$ Ans

Ans-3 Capacitive input Filter

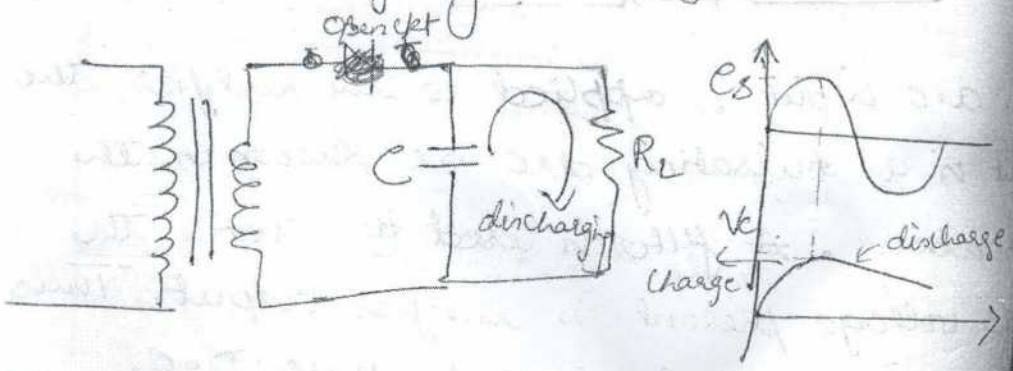
i) Filter with HWR



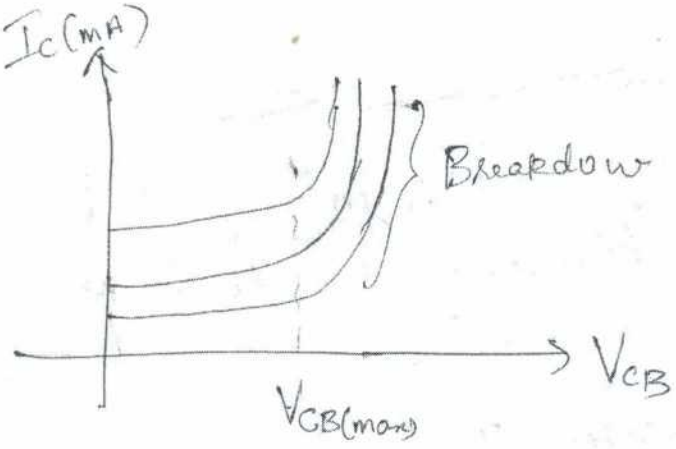


During the +ve half cycle, the input e_s fwd bias the diode D_1. This charges the Capacitor C to peak value of the input i.e

When the input starts decreasing below peak, the diode gets rev biased. b'coz the Cathode is at higher potential & anode is at lower potential. Hence capacitor starts discharging through R_L as shown

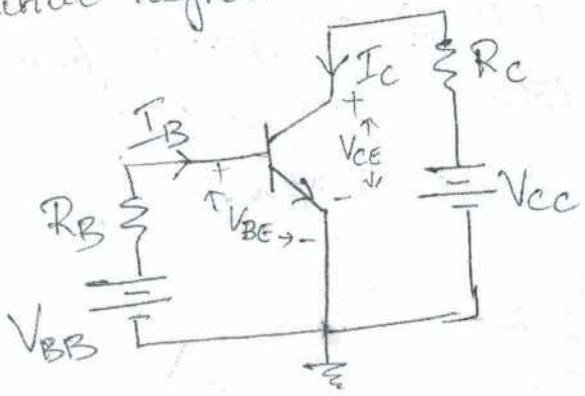


Discharging of capacitor is decided by $R_L C$ time which is very large.

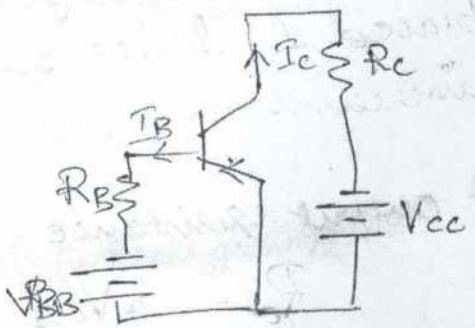


Common Emitter characteristics

Consider an npn transistor in CE mode & active region.

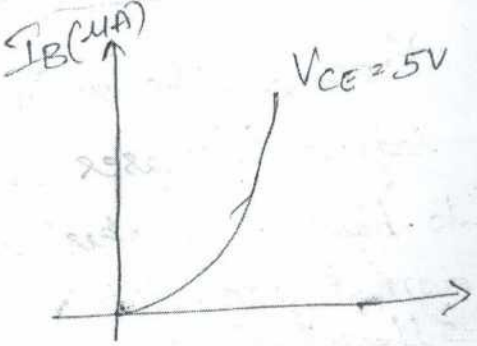


PnP



input characteristics

It is graph of input current (I_B) & input voltage (V_{BE}) keeping output voltage V_{CE} const.

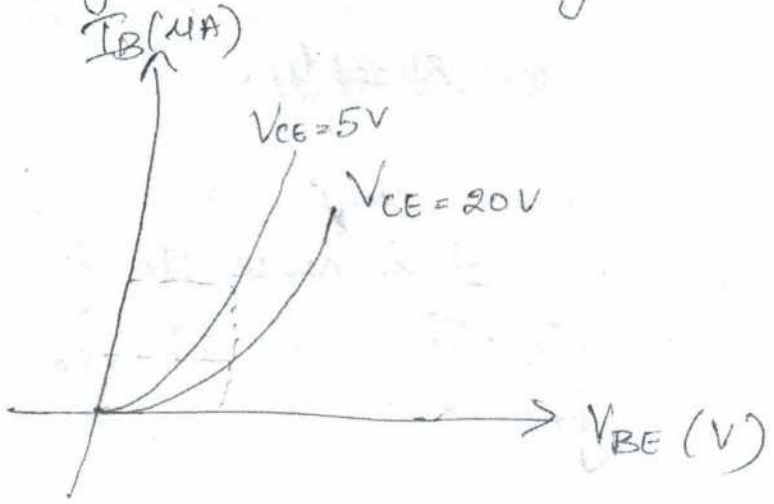


1) Since E-B jn is fwd biased, I_B increases Exponentially with increase in V_{BE}

$\therefore$ I/p resistance $R_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CB} = \text{const}}$

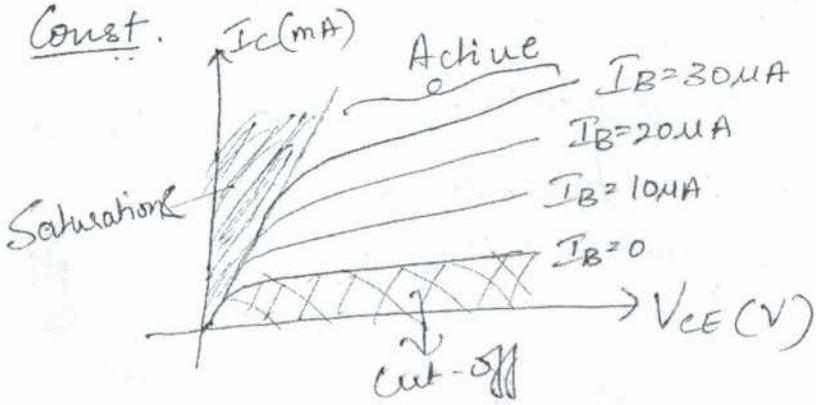
R_i is low ($\because$ fwd bias)

2) As V_{CE} increases (rev bias voltage), Base width decreases due to increase in depletion region of C-B jn. Due to reduced Base width, there are fewer recombinations in base region, thus reducing I_B.



Output characteristics

It is a graph of output current (I_c) & O/P voltage (V_{CE}), keeping I/P current (I_B) const.



1) Output dynamic resistance

$$R_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B = \text{const}}$$

R_o is high (C-B jn is rev bias)

2) Active Region: Since collector jn is reverse biased. As V_{CE} is increased, reverse bias increases. This causes depletion region to spread more in base than in collector, reducing the chance of recombination in the base. hence collector current increases more sharply.

3) Saturation Region: when both E-B jn & C-B jn is fwd biased & hence I_C goes to saturation. The saturation value of V_{CE} is $V_{CE(sat)}$ varies from 0.1V to 0.3V.

4) Cut-off: when input base current is zero, the collector current is reverse leakage current I_{CEO}. The region below $I_B = 0$ is called cut-off region.

5) If the reverse bias voltage increases beyond a certain limit, the breakdown occurs in transistor. This effect is called punch through Effect.

Ans 4 Average D.C load Current (I_{DC})

$I_L = I_m \sin \omega t \quad 0 \le \omega t \le \pi$

$I_L = I_m \sin \omega t \quad \pi \le \omega t \le 2\pi$

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} i_L \cdot d\omega t$$

$$= \frac{2}{2\pi} \int_0^{\pi} i_L \cdot d\omega t$$

$$= \frac{1}{\pi} \int_0^{\pi} I_m \sin \omega t \cdot d\omega t$$

$$= \frac{I_m}{\pi} \left[-\cos \omega t \right]_0^{\pi}$$

$$\boxed{I_{dc} = \frac{2I_m}{\pi}}$$

Average D.C load voltage

$$\boxed{V_{dc} = I_{dc} \times R_L}$$

$$V_{dc} = \frac{2I_m}{\pi} \times R_L$$

Rms value of load Current I_{rms}

$$I_{rms} = \sqrt{\frac{2}{2\pi} \int_0^{\pi} (i_L)^2 \cdot d\omega t}$$

$$= \sqrt{\frac{1}{\pi} \int_0^{\pi} I_m^2 \sin^2 \omega t \cdot d\omega t}$$

$$= \sqrt{\frac{1}{\pi}\int_0^{\pi} \frac{1-\cos 2\omega t}{2} \cdot d\omega t}$$

$$\boxed{I_{rms} = \frac{I_m}{\sqrt{2}}}$$

R.m.s value of load voltage

$$\boxed{E_{rms} = I_{rms} R_L}$$

$$E_{rms} = \frac{I_m}{\sqrt{2}} R_L$$

D.C power output P_{DC}

$$\boxed{P_{DC} = V_{dc} \cdot I_{dc}}$$

$$P_{DC} = \frac{2I_m}{\pi} \times R_L \times \frac{2I_m}{\pi}$$

$$= \frac{4I_m^2}{\pi^2} \times R_L$$

A.C power input P_{AC}

$$\boxed{P_{AC} = I_{rms}^2 \times (R_f + R_L + R_s)}$$

$$P_{AC} = \frac{I_m^2}{2}(R_f + R_L + R_s)$$

η Efficiency of Rectifier

$$\eta = \frac{P_{DC}}{P_{AC}} = \frac{\frac{4}{\pi^2} I_m^2 R_L}{\frac{I_m^2}{2}(R_f + R_L + R_S)}$$

$$= \frac{8 R_L}{\pi^2 R_f + R_L + R_S}$$

$\because R_f + R_S \ll R_L$.

$$\% \eta = \frac{8}{\pi^2} \times 100 = 81.2\%$$

Ripple factor (γ).

$$\gamma = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1}$$

$$= \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.48$$

PIV := $-2E_m$

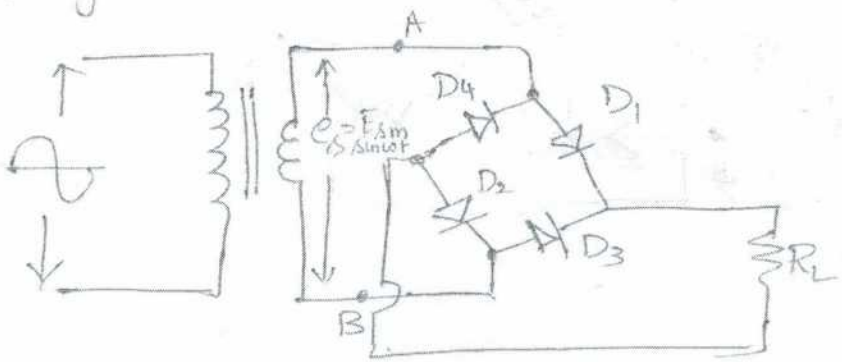
TUF → Refer class notes.

→ Learn adv & disadv of HWR & FWR.

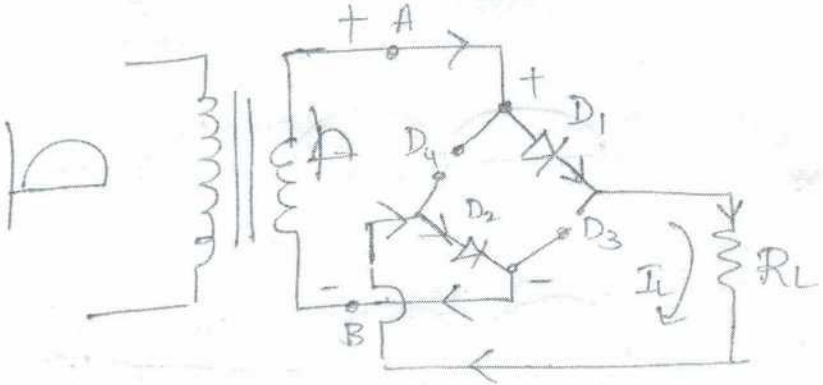
→ Solve numericals.

Bridge Rectifier

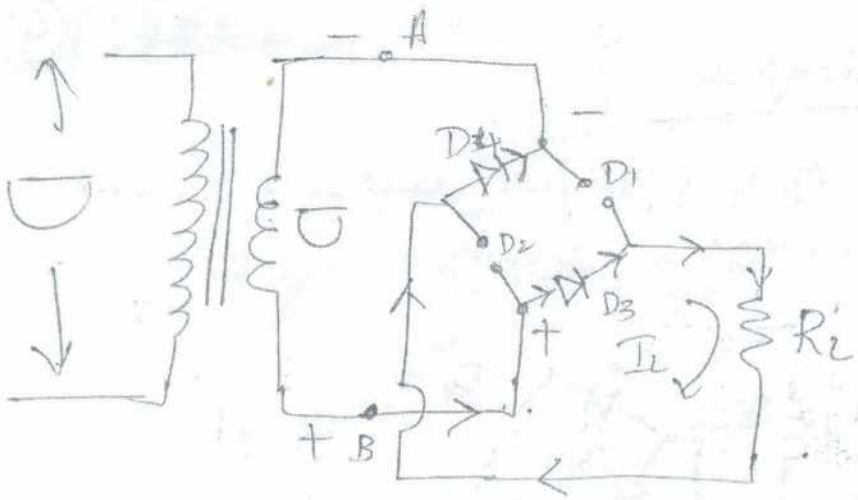
Bridge Rectifier is a full-wave rectifier ckt using 4 diodes as shown.

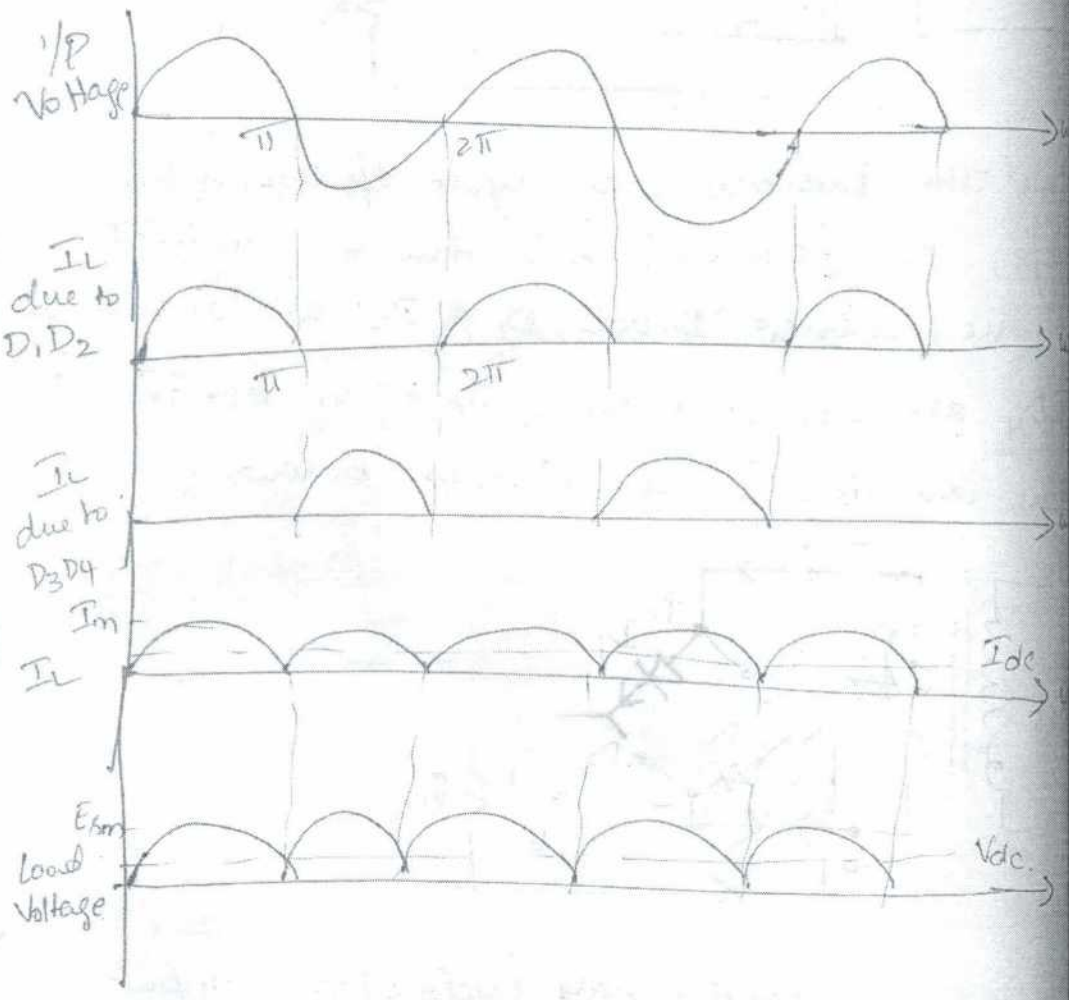


During the positive half cycle of a.c input voltage, the terminal A is +ve & terminal B is -ve., hence Diode D_1 & D_2 are conducting D_3 & D_4 are non-conducting i.e open ckt. The current direction is as shown below



During the negative half cycle of a.c input voltage, the terminal A is -ve & terminal B is +ve, hence Diode D_3 & D_4 are conducting, D_1 & D_2 are non-conducting i.e open ckt. The current direction is as shown below





$$I_m = \frac{E_{sm}}{R_s + 2R_j + R_L}$$

$2R_j$ ← Since during each half cycle two diodes are conducting

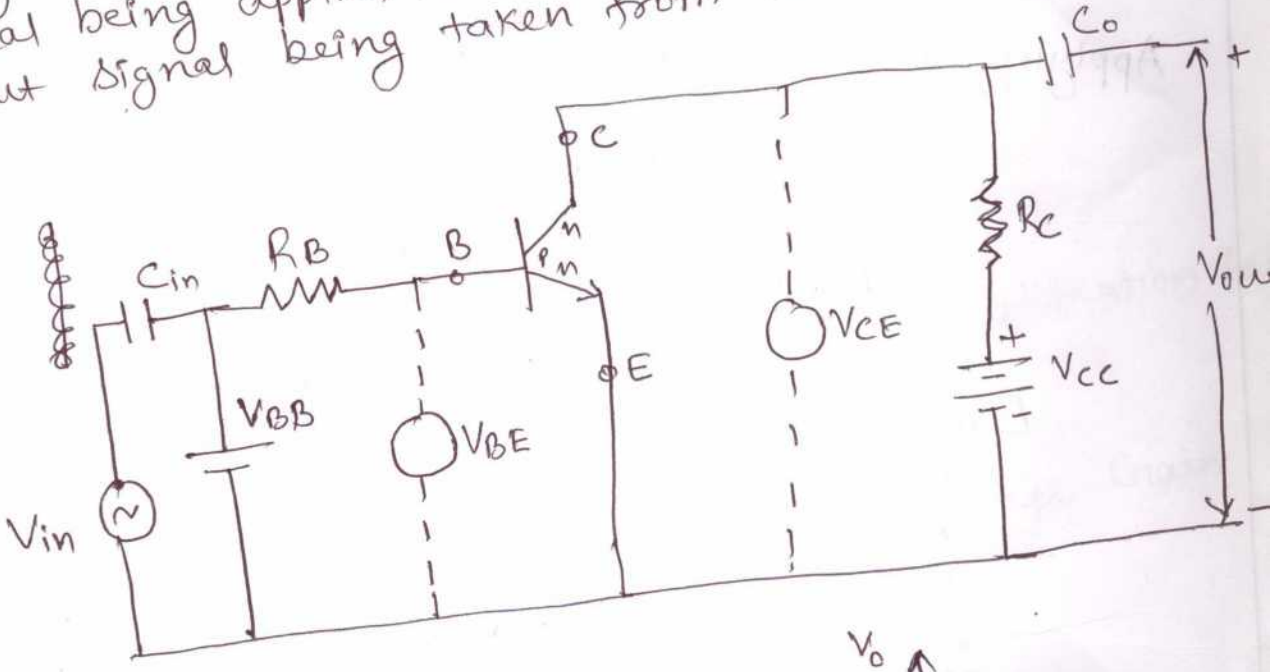
Q5 (a) Show that CE mode transistor act as a Voltage amplifier?

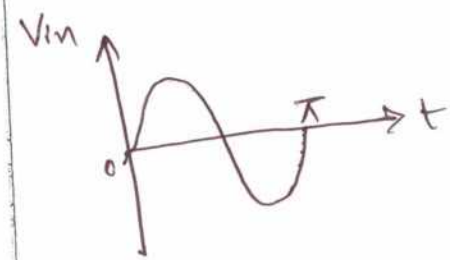
Ans — * The amplifier Circuit that is formed using a CE Configured transistor Combination is Called as CE amplifier.

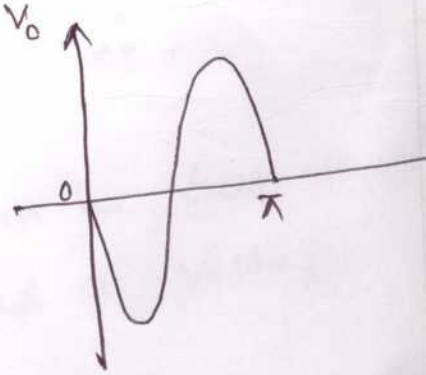
* The Process of increasing the signal strength is Called as Amplification.

Construction —

The Common emitter amplifier Circuit using NPN transistor is shown below, the input signal being applied at emitter base Junction and the output signal being taken from Collector base Junction







The emitter base Junction is forward Biased by V_{BB} and Collector base Junction is Reverse biased by V_{CC}.

Operation -

When no i/p is applied, the Quiescent Condition are formed and no output is present. When positive half of the signal is being applied the Voltage between base and emitter V_{be} is increased because it is already positive with repect to gnd.

As forward bias increases, the base current too increases accordingly. Since $I_C = \beta I_B$, the Collector Current increases as well.

Applying KVL to Input Loop -

$$V_{BB} = R_i i_B + V_{BE}$$

$$\Delta V_{BB} = R_i \Delta i_B + \Delta V_{BE}$$

ΔV_{BE} is very small can be neglected.

and $\Delta V_{BB} = \Delta V_i$

$$\therefore \boxed{\Delta V_i = R_i \Delta i_B}$$

$$\frac{\Delta V_i}{\Delta i_B}$$

Applying KVL on o/p loop -

$V_{CC} = i_C R_C + V_{CE}$

V_{CE} = o/p voltage

$\therefore V_{CC} = i_C R_C + V_o$

$V_o = V_{CC} - i_C R_C$

$V_{CC} \neq \Delta i_C R_C + \Delta V_o$

$\Delta V_o = 0 - \Delta i_C R_C$

$\therefore \boxed{\Delta V_o \neq V_{CC} + \Delta i_C R_C}$

$\therefore \boxed{\Delta V_o = -\Delta i_C R_C}$

A_V = Voltage Gain $= \frac{\Delta V_o}{\Delta V_i}$

$\therefore A_V = \frac{-\Delta i_C R_C}{\Delta i_B R_B}$

$\frac{\Delta i_C}{\Delta i_B} = \beta_{ac}$ (Current amplification factor)

$\therefore \boxed{A_V = -\beta_{ac}\left(\frac{R_C}{R_B}\right)}$ Voltage Gain

$\boxed{A_i = \beta_{ac}}$ Current Gain.

Hence, it can be seen that CE mode transistor works as a Voltage Amplifier.

CMR

9b) i) Alpha (α) :- It is the ratio of Collector Current to Emitter Current. It gives the Current gain in Common base Configuration.

Beta (β) :⇒ It is the ratio of Collector Current to base Current. It gives the Current Gain in Common Emitter Configuration.

$$\therefore \quad \boxed{\alpha = \frac{I_C}{I_E}} \quad \text{and} \quad \boxed{\beta = \frac{I_C}{I_B}}$$

Relationship Between α & β :⇒

We Know

$$I_E = I_C + I_B$$

$$\therefore \quad I_B = I_E - I_C$$

Divide by I_C both side

$$\frac{I_B}{I_C} = \frac{I_E}{I_C} - 1$$

$$\frac{1}{\beta} = \frac{1}{\alpha} - 1$$

$$\therefore \quad \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

As we know $\alpha = \frac{I_C}{I_E}$

$\therefore \quad \alpha = \frac{I_C}{I_B + I_C}$ $\quad (As\ I_E = I_C + I_B)$

↳ Divide Num & Deno by I_B

$$\alpha = \frac{I_C/I_B}{I_B/I_B + I_C/I_B}$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

(ii) Given $I_C = 1mA$ and $I_B = 25\mu A$

$$\therefore \quad \beta = \frac{I_C}{I_B}$$

$$= \frac{1 \times 10^{-3}}{25 \times 10^{-6}}$$

$$\boxed{\beta = 40} \quad \text{Ans}$$

As we know

$$\alpha = \frac{\beta}{1+\beta} = \frac{40}{1+40} = \frac{40}{41}$$

$$\boxed{\alpha = 0.9756} \quad \text{Ans}$$

CMR

S01.6 ⇒

$$\frac{N_2}{N_1} = \frac{E_{s(rms)}}{E_{p(rms)}}$$

$$\frac{1}{4} = \frac{E_{s(rms)}}{230V}$$

$$E_{s(rms)} = \frac{230}{4} = 57.5\ V$$

$$E_{sm} = \sqrt{2} \times E_{s(rms)} = 57.5 \times \sqrt{2}$$

$$\boxed{E_{sm} = 81.317\ V}$$

$$I_m = \frac{E_{sm}}{R_s + R_f + R_f}$$

Given $R_L = 600\Omega$ $R_f = 20\Omega$ $R_s = 0$

$$I_m = \frac{81.317}{600+20}$$

$$\boxed{I_m = 0.1312\ Amp}$$

$$I_{DC} = \frac{2I_m}{\pi}$$

$$\boxed{I_{DC} = 0.0835\ A}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}^2} = 0.0122\ A$$

$$\boxed{I_{rms} = 0.0122\ A}$$

(I) $P_{DC} = I_{DC}^2 \times R_L$

$$\boxed{P_{DC} = 4.1834\ W}$$

$$P_{ac} = I_{rms}^2 (R_f + R_L)$$

$$\boxed{P_{ac} = 5.339\ W}$$

(II)

Efficiency

$$\eta\% = \frac{P_{DC}}{P_{ac}} \times 100$$

$$= \frac{4.1834}{5.339} \times 100$$

$$\boxed{\eta = 78.35\%}$$

(III) $PIV = 2E_{sm}$

$= 2 \times 81.317$

$$\boxed{PIV = 162.634V}$$

(IV) Ripple frequency $= 2f$

I/p freq $= 50\ Hz$ (Given)

$\therefore$ Ripple freq $= 2 \times 50$

$= 100\ Hz$

(IV) Ripple factor $= \sqrt{\frac{\pi^2}{8} - 1}$

$= 0.48$

X ——— X ——— X