CMR
INSTITUTE OF
TECHNOLOGY

USN

Internal Assesment Test - II

Sub:	**OPERATIONAL AMPLIFIERS AND LINEAR ICs**							Code:	15EE46
Date:	17/04/2018	Duration:	90 mins	Max Marks:	50	Sem:	4th	Branch:	EEE

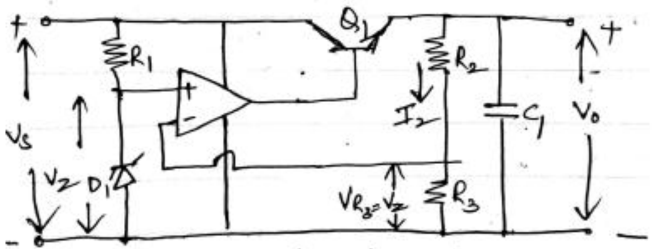
Answer Any FIVE FULL Questions

		Marks	OBE	
			CO	RBT
1	Discuss the operation of a voltage follower regulator with the help of circuit diagram. Define line regulation and load regulation for a voltage regulator.	10	CO6	L2
2	Demonstrate the operation of triangular/rectangular signal generator with a neat circuit diagram and required waveforms.	10	CO5	L3
3	Design a RC phase shift oscillator to generate a sinusoidal output of 1000Hz and supply voltage ±15V using uA 741 op-amp. Explain the method to attain output amplitude in RC phase shift oscillator with circuit diagram.	10	CO5	L3
4	Design a non inverting Schmitt trigger to have UTP=+2V and LTP=-3V using uA741 Op-amp with supply voltage Vcc=±15V.	10	CO4	L3
5	Explain the circuit of a full wave precision rectifier using half wave rectifier and summing circuit. Demonstrate the input and output waveforms.	10	CO3	L2
6	Demonstrate the operation of peak clipper using Zener diodes and positive clipper with positive reference voltage with circuit diagram and necessary waveforms.	10	CO3	L2
7	Demonstrate the operation of inverting Schmitt trigger with a neat circuit diagram, waveforms and input-output characteristics.	10	CO4	L3

1.

Adjustable voltage regulator

→ o/p V greater than zener diode voltage.



$V_{R_3} = V_Z$ $\quad$ $V_{R_3} > V_Z$ o/p will fall.

$V_0 \downarrow$ until $V_{R_3} = V_Z$.

Op-amp is error amplifier because it amplifies error is to keep output to desired level.

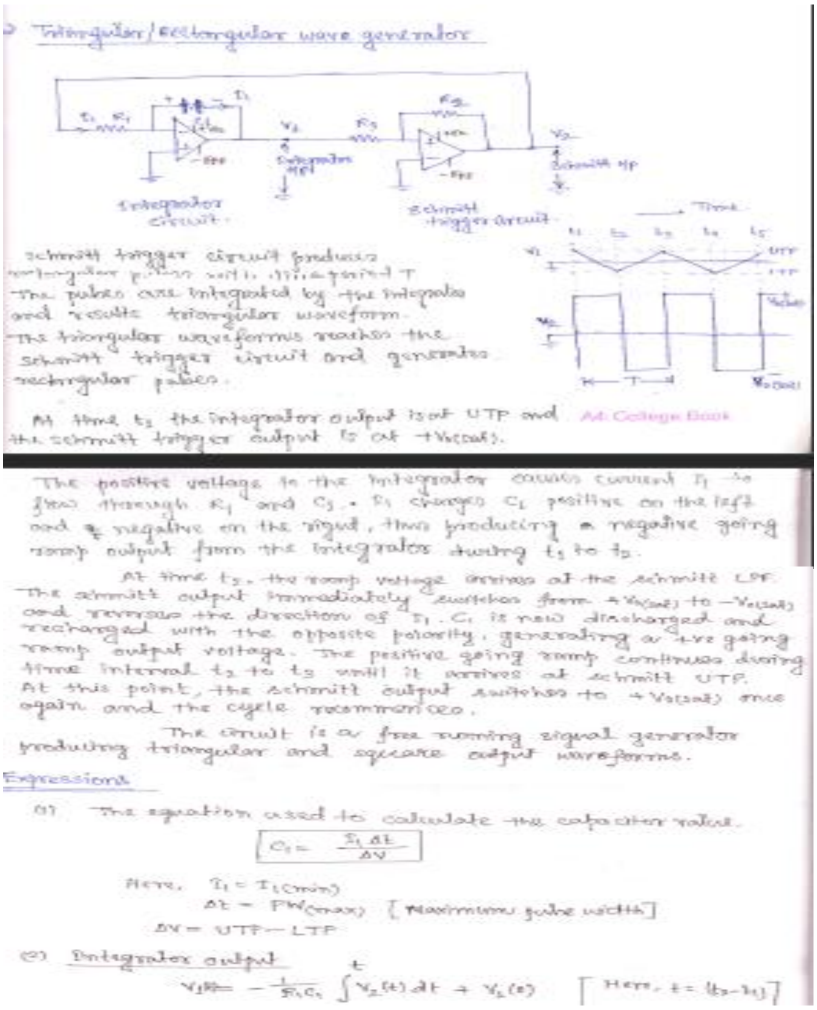
$V_{R_3} = V_Z$

$$V_Z = \frac{V_0 \times R_3}{R_2 + R_3}$$

$$V_0 = \frac{V_Z (R_2 + R_3)}{R_3}$$

$$\Delta V_0 = \frac{\Delta V_S Z_Z}{R_1} \left(\frac{R_2 + R_3}{R_3} \right)$$

2.



→ Triangular/Rectangular wave generator

Schmitt trigger circuit produces rectangular pulses with time period T
- The pulses are integrated by the integrator and results triangular waveform.
- The triangular waveforms reaches the schmitt trigger circuit and generates rectangular pulses.

At time t_1 the integrator output is at UTP and the schmitt trigger output is at $+V_{o(sat)}$.

The positive voltage to the integrator causes current I_1 to flow through R_1 and C_1. I_1 charges C_1 positive on the left and negative on the right, thus producing a negative going ramp output from the integrator during t_1 to t_2.

At time t_2, the ramp voltage arrives at the schmitt LTP. The schmitt output immediately switches from $+V_{o(sat)}$ to $-V_{o(sat)}$ and reverses the direction of I_1. C_1 is now discharged and recharged with the opposite polarity, generating a +ve going ramp output voltage. The positive going ramp continues during time interval t_2 to t_3 until it arrives at schmitt UTP. At this point, the schmitt output switches to $+V_{o(sat)}$ once again and the cycle recommences.

The circuit is a free running signal generator producing triangular and square output waveforms.

Expressions

(1) The equation used to calculate the capacitor value.

$$\boxed{C_1 = \frac{I_1 \Delta t}{\Delta V}}$$

Here, $I_1 = I_{1(min)}$

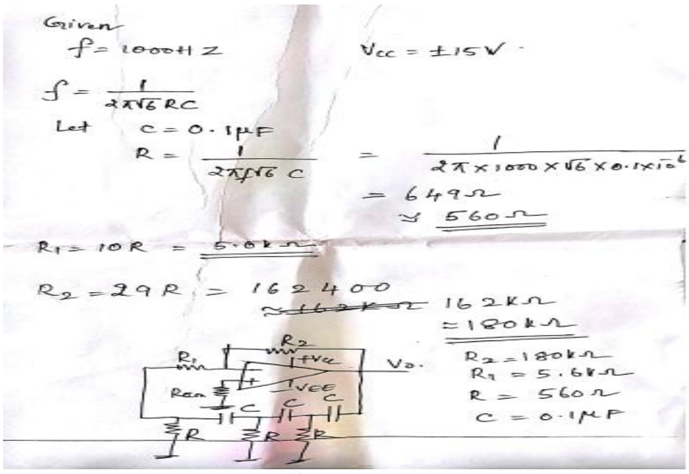
$\Delta t = PW_{(max)}$ [Maximum pulse width]

$\Delta V = UTP - LTP$

(2) Integrator output

$$V_1(t) = -\frac{1}{R_1 C_1}\int^{t} V_2(t)\,dt + V_1(0) \qquad \left[\text{Here, } t = (t_2 - t_1)\right]$$

3.



Given

$f = 1000\,Hz$ $V_{cc} = \pm 15V$.

$$f = \frac{1}{2\pi\sqrt{6}RC}$$

Let $C = 0.1\mu F$

$$R = \frac{1}{2\pi f\sqrt{6}\,C} = \frac{1}{2\pi \times 1000 \times \sqrt{6} \times 0.1 \times 10^{-6}}$$

$= 649\Omega$

$\simeq \underline{\underline{560\Omega}}$

$R_1 = 10R = \underline{\underline{5.6k\Omega}}$

$R_2 = 29R = 162400$

$\simeq$ ~~162kΩ~~ $162k\Omega$

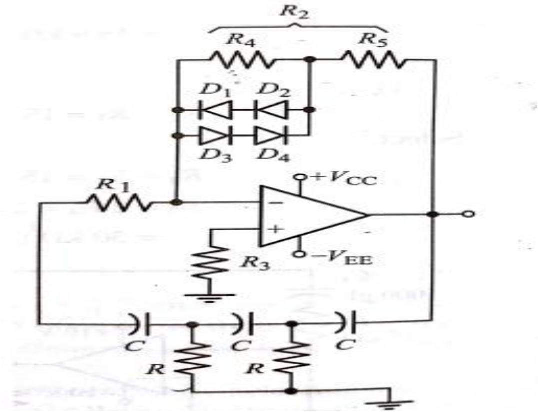
$\simeq \underline{\underline{180k\Omega}}$

$R_2 = 180k\Omega$

$R_1 = 5.6k\Omega$

$R = 560\Omega$

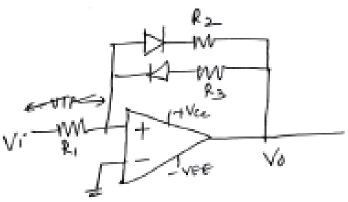
$C = 0.1\mu F$



4.

4) UTP = +2V   LTP = −3V

$R_1 = \frac{UTP}{I_1} = \frac{2}{500\mu A} = 4 k\Omega$ $\underline{\underline{(3.9 k\Omega)}}$



$UTP = \frac{(V_o - V_D) \times R_1}{R_2}$

$R_2 = \frac{(V_{sat} - V_D) \times R_1}{UTP} = \frac{(14 - 0.7) \times 3.9 \times 10^3}{2}$

$= 25 k\Omega$ $\underline{\underline{(27 k\Omega)}}$

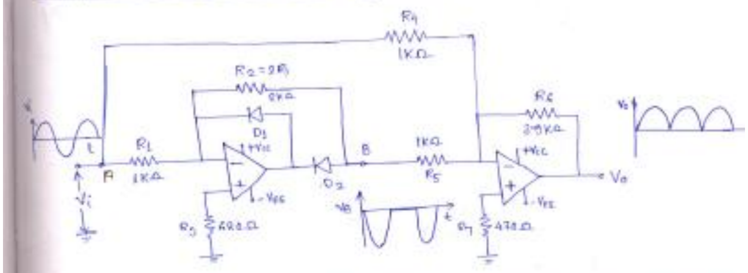
$R_3 = \frac{(V_{sat} - V_D) \times R_1}{LTP} = \frac{(14 - 0.7) \times 3.9 \times 10^3}{3} = 17 k\Omega$

$\underline{\underline{\approx 18 k\Omega}}$

5.

Precision Full-wave Rectifiers

Half-wave Rectifier and Summing Circuit



The above circuit is a combination of half-wave rectifier with gain = 2 and an inverting adder with gain = 3.9

During +ve half-cycle

Voltage at terminal A = +Vi
while that at terminal B is −2Vi.
[Diode D₁ is off and D₂ is on]

~~During~~ The output of the summing circuit, with $R_4 = R_5$

$$V_o = -\frac{R_6}{R_4}(V_A + V_B)$$
$$= -\frac{R_6}{R_4}(V_i - 2V_i)$$
$$= -\frac{R_6}{R_4}(-V_i) = \frac{R_6}{R_4} V_i$$

During −ve half-cycle

$V_A = -V_i$
$V_B = 0$ as D_1 is on and D_2 is off.

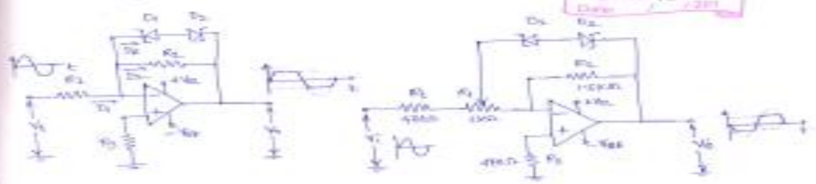
Consequently the output is,

$$V_o = -\frac{R_6}{R_4}(V_A + V_B) = -\frac{R_6}{R_4}(-V_i + 0)$$
$$\boxed{V_o = +\frac{R_6}{R_4} V_i}$$

So, it can be seen that

6.

Limiting circuits – Peak clipper



Back to back zener diodes are used to clip-off the peaks of the output voltage waveform. One diode is forward biased and the other diode is in reverse breakdown region when the output voltage is greater than $(V_F + V_Z)$. So, the output voltage cannot exceed $\pm(V_F + V_Z)$. As long as the output voltage is less than this limit, the circuit behaves as inverting amplifier, unaffected by the diodes.

The second circuit is a modification of the first circuit where a resistor R_4 is connected in series with R_1. Using R_4 we can change the limiting voltage.

Suppose $R_1 = R_4 = R_2$ and $(V_Z + V_F) = 4V$. With moving the contact at the right side of R_4,

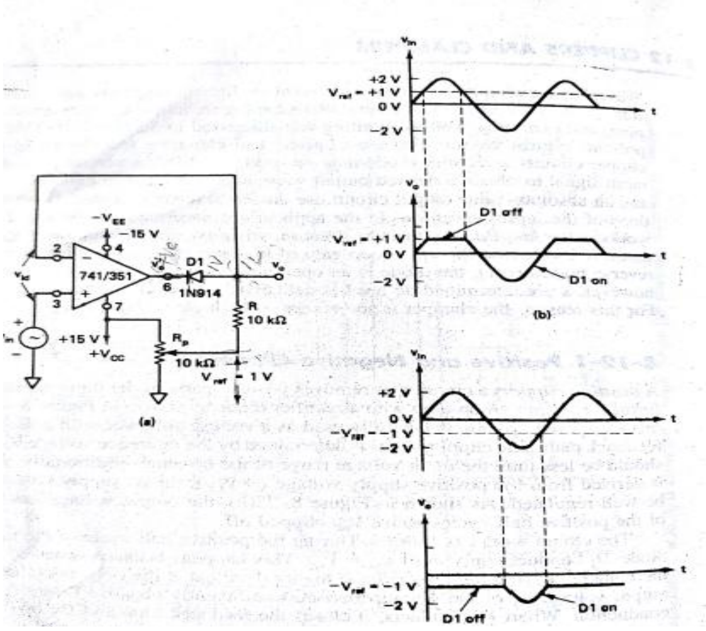
$$V_{o(max)} = V_Z + V_F = \pm 4V \quad ①$$

With moving the contact at the left of R_4,

$$V_{R2} + V_{R4} = V_Z + V_F = \pm 4V$$

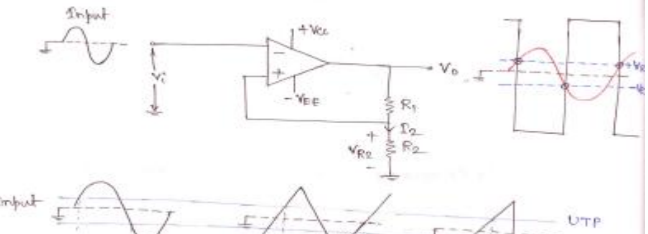
With $R_2 = R_4$, $V_{R2} = V_{R4} = \pm 2V$

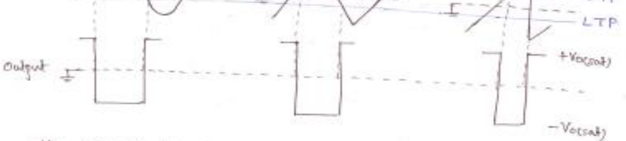
Giving, $\boxed{V_{o(max)} = \pm 2V = V_{R2}}$



7.

Inverting Schmitt trigger circuit





The circuit looks like a non-inverting amplifier except for

(1) The input is applied to the inverting amplifier.

(2) The feedback is connected to the non-inverting terminal.

The voltage at the non-inverting input is–

$$V_{R2} = \frac{V_o \cdot R_2}{R_1 + R_2}$$

when, $V_0 = +V_{o(sat)}$, $V_{R2} = +ve$

$V_0 = -V_{o(sat)}$, $V_{R2} = -ve$

For example, if $V_0 = +11$ V and $R_2 = R_1$

then, $V_{R2} = +5.5$ V

If $V_0 = -11$ V and $R_2 = R_1$ then $V_{R2} = -5.5$ V

So, with zero input voltage, the non-inverting input terminal is +ve voltage, so output remains at its positive saturation voltage.

The output will switch from the positive saturation level to negative saturation voltage when the voltage at the inverting input terminal is raised above the voltage level at the non-inverting input terminal i.e. V_{R2}.

Once the output voltage is $-V_{o(sat)}$ then V_{R2} is negative. The output changes from $-V_{o(sat)}$ to $+V_{o(sat)}$ when the input becomes lower than $-V_{R2}$ volt. This is positive feedback and it causes the output to move rapidly from one saturation level to another.

Observation

If $V_{o(sat)} = 11$ volt and $R_1 = R_2$ then $V_{R2} = +5.5$ volt.

$V_{o(sat)} = -11$ volt and " " $V_{R2} = -5.5$ V

The output changes from one saturation level to another when the input crosses the voltages $+V_{R2}$ and $-V_{R2}$. These two points are known as upper trigger and lower trigger point respectively.

In this example, UTP = +5.5 volt, LTP = −5.5 volt.

Input/output characteristics

Typical input/output or transfer characteristics of an op-amp inverting schmitt trigger circuit is shown.

(1) When V_i is raised to the UTP, the output switches from $+V_{o(sat)}$ to $-V_{o(sat)}$ → (Point a to b)

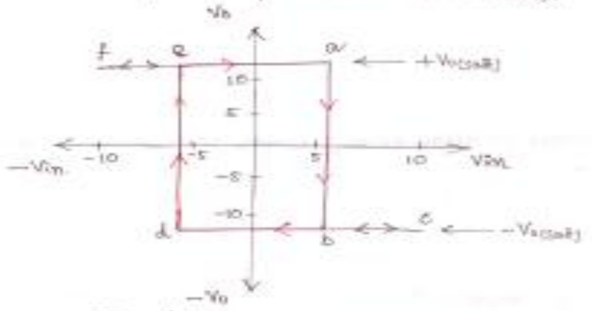
(2) V_i is above the UTP, the output remains at $-V_{o(sat)}$. → Point b to c

(3) While the input is being reduced from UTP to the LTP, the output remains at $-V_{o(sat)}$ → Point b to d

(4) When V_i equals the LTP, the output rapidly switches from $-V_{o(sat)}$ to $+V_{o(sat)}$ → Point d to e

(5) Any further decrease of V_i below LTP, maintains the output voltage at $+V_{o(sat)}$ → Point e to f

(6) Till UTP the output voltage remains at $+V_{o(sat)}$.



Transfer characteristics of inverting schmitt trigger circuit.

The difference between the UTP and LTP is referred to as hysteresis. For zero crossing detector (ZCD) have UTP and LTP equal, so, they have zero hysteresis.

Schmitt trigger circuit design

The current through resistors R_1 and R_2 is first calculated as much higher than input bias current.

$$R_2 = \frac{\text{Trigger voltage}}{I_2}$$

$$R_1 = \frac{V_0 - (\text{Trigger voltage})}{I_2}$$

where $I_2 = 100 I_{B\,max}$